



# EASYLOGIX.DE

**CAD/CAM**  
**for electronics**



## **DFM/DRC**

- *Solder Paste*
- *Solder Mask*
- *Signal*
- *Drill*
- *Component*
- *Component Pins*

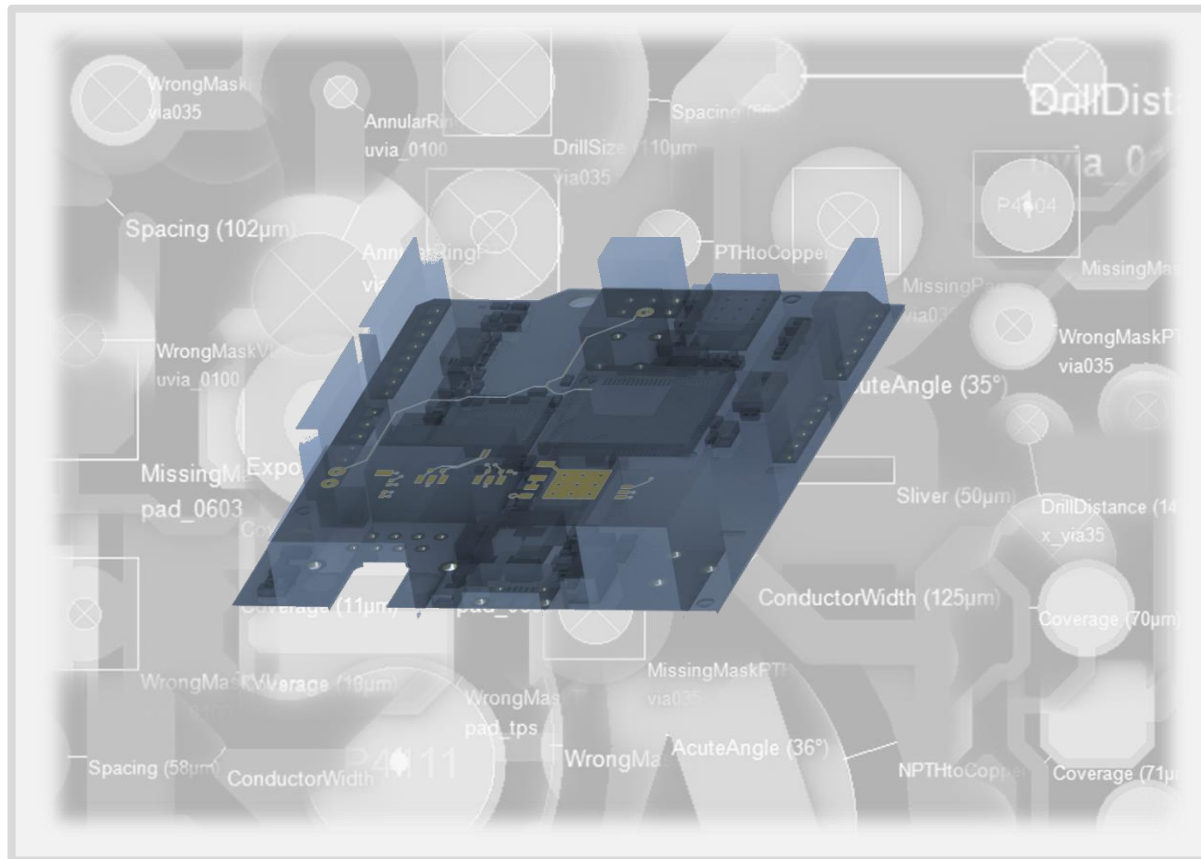
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# Design for Manufacturing

## DFM

DRC Rules to increase quality and reduce costs.  
The rules apply to **PCB Manufacturing** and **Assembly**



# Design for Manufacturing

## DFM

Data Formats

Workflow

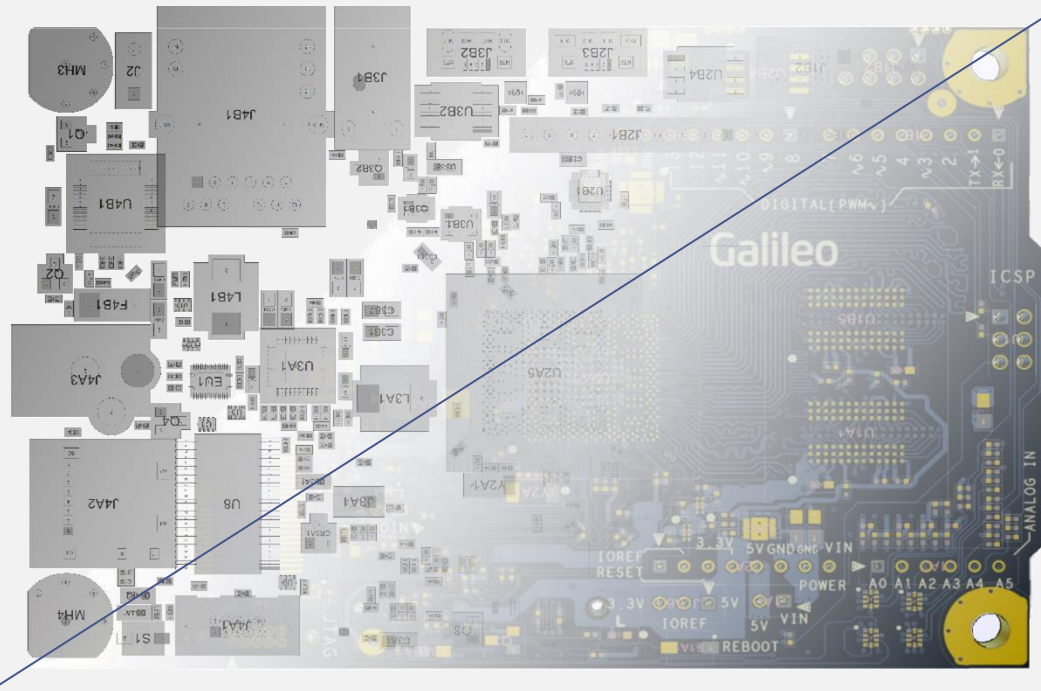
Preparations

Results

- Copper
- Mask
- Drills
- Components

There are many checks requiring the knowledge of both, component and Bare Board information.

PCB Assembly



PCB Bare Board

# Design for Manufacturing

## DFM

Data Formats

Workflow

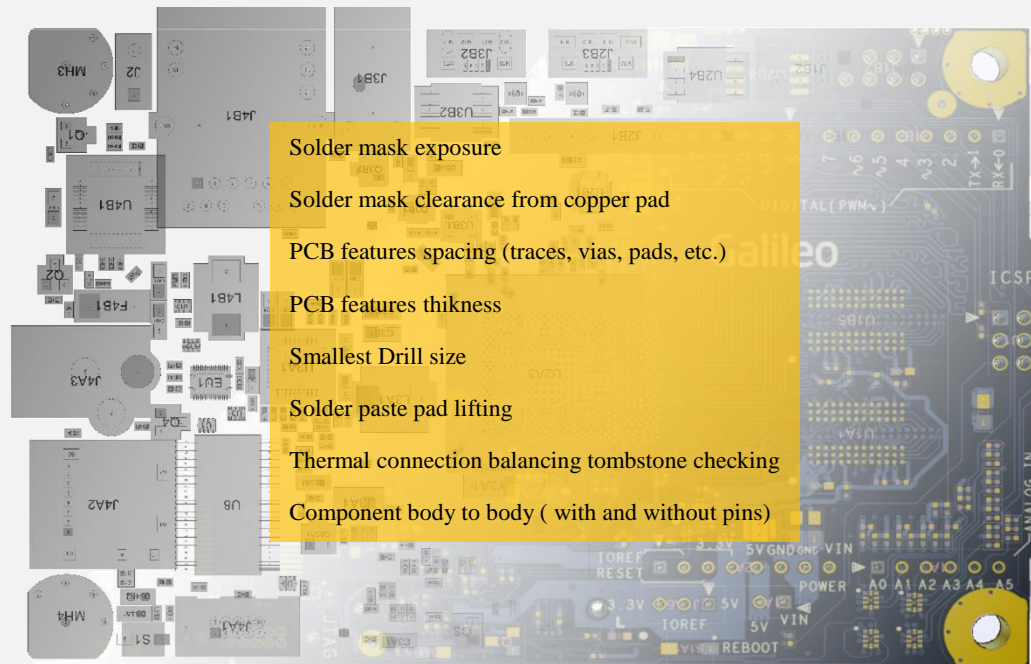
Preparations

Results

- Copper
- Mask
- Drills
- Components

There are many checks requiring the knowledge of both, component and Bare Board information.

## PCB Assembly



PCB Bare Board

# DFM – Data Formats

DFM

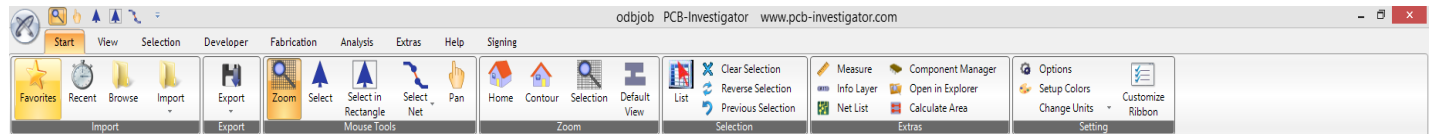
Data Formats

Workflow

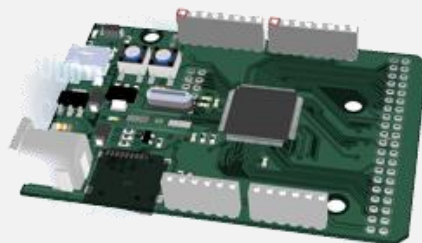
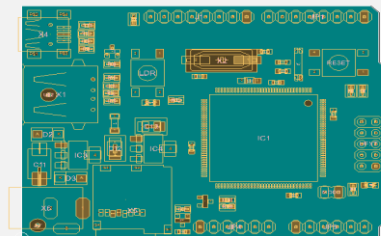
Preparations

Results

- Copper
- Mask
- Drills
- Components



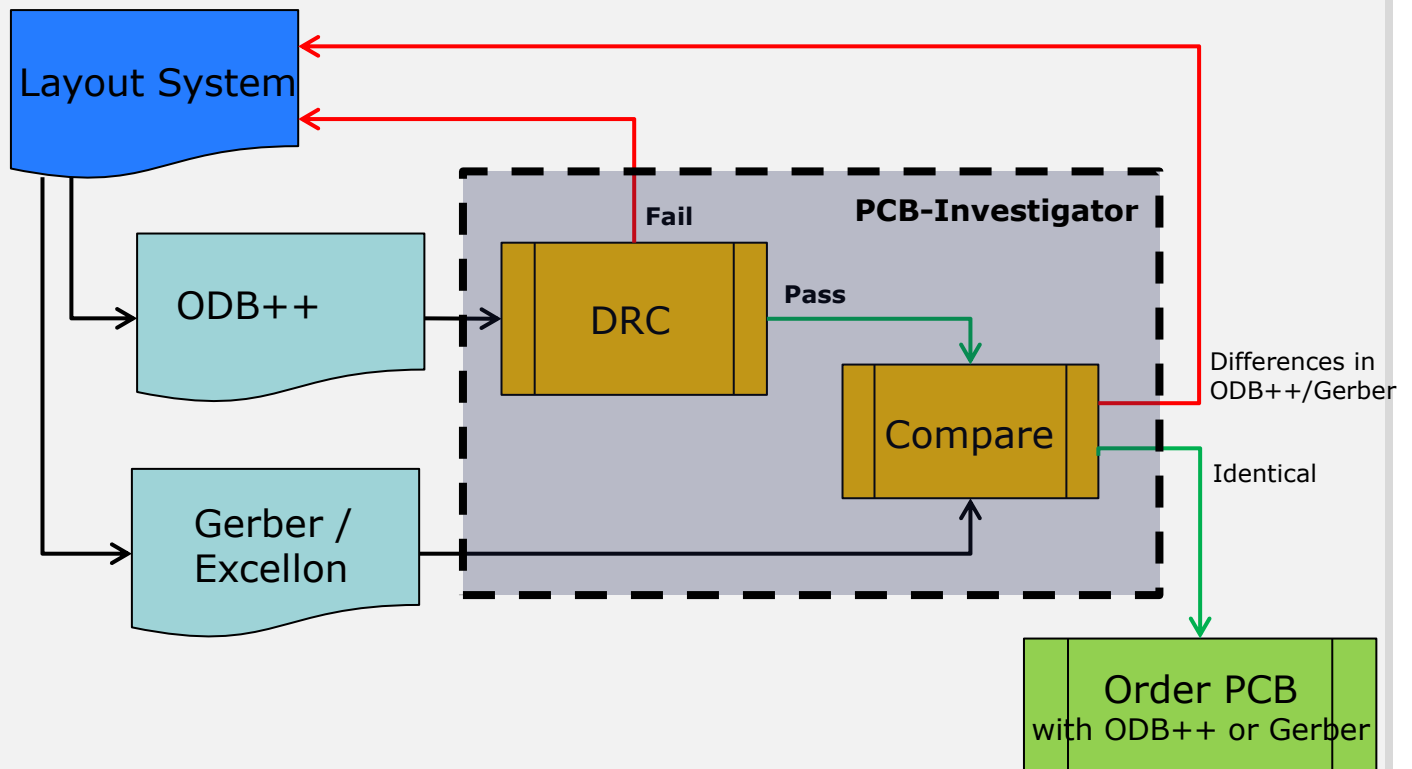
Format 2D	Import	Export
ODB++	Yes	Yes
IPC-2581	Yes	Yes
GenCAD 1.4	Yes	Yes
EAGLE „ULP“	Yes	No
Gerber274x	Yes	Yes
Excellon	Yes	No
Sieb&Meyer	Yes	No
DXF	Yes	Yes
PDF	Yes	Yes



Format 3D	Import	Export
VRML	Yes	Yes
Obj	Yes	Yes
X3D	Yes	Yes
XAML	Yes	Yes
IDF 2.0/3.0	Yes	Yes

# DFM – Workflow

**DRC check should be done on ODB++ to utilize all information integrated in the ODB++ structure**



# DFM – Preparations / Setup

DFM

Data Formats

Workflow

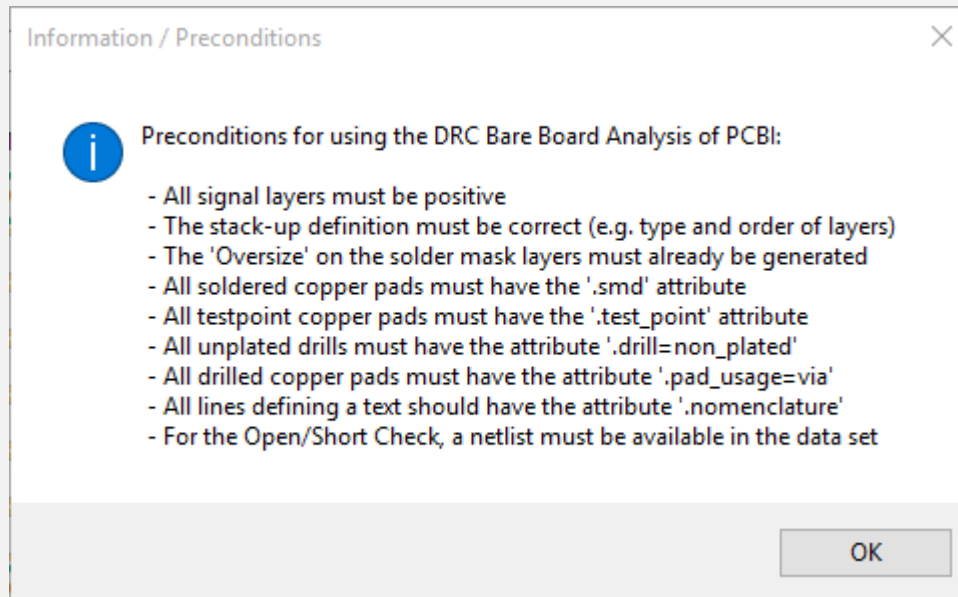
Preparations

Results

- Copper
- Mask
- Drills
- Components

## Is data preparation necessary?

In case your ECAD System Library does not add the proper attributes to the design, it is possible to add the missing attributes with a small script to prepare your PCB-Data.



# DFM – Preparations / Setup

DFM

Data Formats

Workflow

Preparations

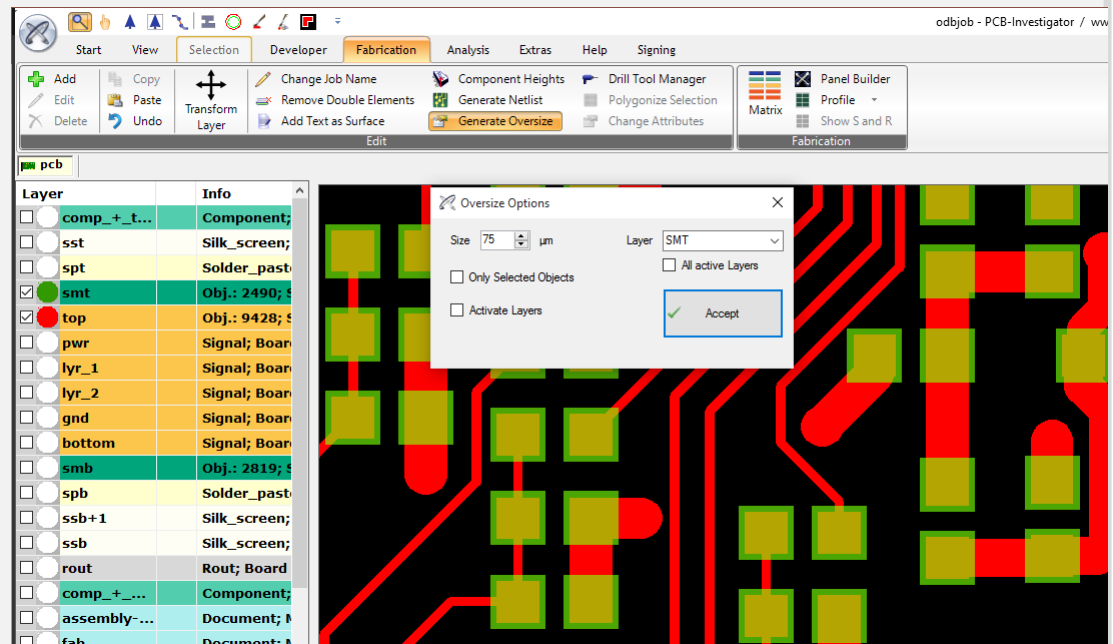
Results

- Copper
- Mask
- Drills
- Components

## Is data preparation necessary?

Depending of the used library, the Solder Mask Oversize is already applied in the data or must be generated with PCB-Investigator.

The Solder Mask oversize is used to make sure, that all soldering pads are free of lacquer, when taking the tolerances of manufacturing into account.





# DFM – Preparations / Setup

DFM

Data Formats

Workflow

Preparations

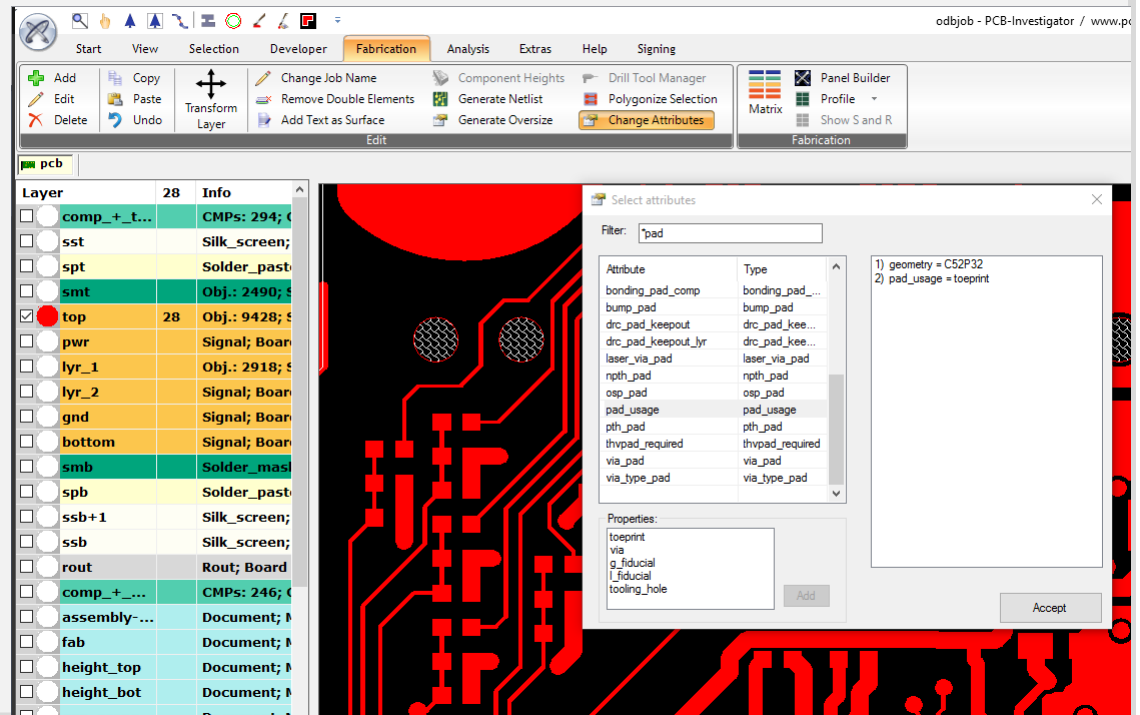
Results

- Copper
- Mask
- Drills
- Components

## Is data preparation necessary?

Preparing PCB fabrication data from Gerber, Excellon Sieb&Meyer

Gerber data does not include information about the type or purpose of the files. This information must be added.



# DFM – Preparations / Setup

DFM

Data Formats

Workflow

Preparations

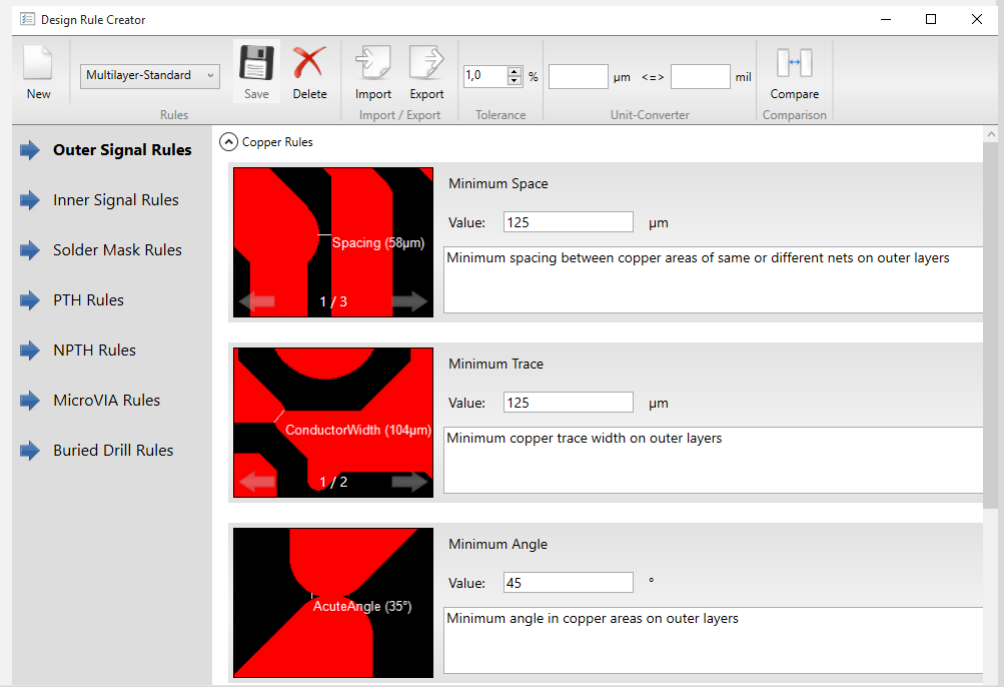
Results

- Copper
- Mask
- Drills
- Components

## Is data preparation necessary?

The DRC Rule File Manager let you set up different categories of PCB types, like standard, advanced, HDI, SBU or any other used technology

Creating rule files is supported by the rule file editor, which creates a XML file to prepare and exchange setups



# DFM – Preparations / Setup

DFM

Data Formats

Workflow

Preparations

Results

- Copper
- Mask
- Drills
- Components

## Is data preparation necessary?

The created rule sets can easily be compared to find all different check values and characteristics of a certain rule set.

All different values between two selected rule sets are highlighted

Compare Rule Sets			
Multilayer-Standard		Multilayer-HighEnd	
Rule	Multilayer-Standard	Multilayer-HighEnd	Description
<b>Outer Signal Rules</b>			
Minimum Space	125 µm	100 µm	Minimum spacing between copper areas of same or different nets on outer layers
Minimum Trace	125 µm	100 µm	Minimum copper trace width on outer layers
Minimum Angle	45 °	45 °	Minimum angle in copper areas on outer layers
Mask Clearance for SMD Pads	75 µm	50 µm	Minimum needed solder mask clearance around SMD pads (smd Attribute)
Mask Clearance for Testpoint Pads	75 µm	50 µm	Minimum needed solder mask clearance around test point pads (test_point Attribute)
<b>Inner Signal Rules</b>			
Minimum Space	125 µm	100 µm	Minimum spacing between copper areas of same or different nets on inner layers
Minimum Trace	125 µm	100 µm	Minimum copper trace width on inner layers
Minimum Angle	45 °	45 °	Minimum angle in copper areas on inner layers
<b>Solder Mask Rules</b>			
Distance to Copper	75 µm	50 µm	Minimum distance from the solder mask opening to surrounding copper
Minimum Space	70 µm	70 µm	Minimum spacing between solder mask clearances (=smallest solder resist fillet)
Minimum Trace	70 µm	70 µm	Minimum width of solder mask clearances
Minimum Angle	45 °	45 °	Minimum angle in solder mask clearances
<b>PTH Rules</b>			
Mask Clearance for PTHs	75 µm	50 µm	Minimum needed solder mask clearance for plated through holes
Mask Clearance for PTH-Pads	75 µm	50 µm	Minimum needed solder mask clearance for plated through hole copper pads
Accept masks smaller as PTH-Pad	on	on	If active, mask clearances which are smaller than the PTH-Pad are not reported
Annular Ring on Outer Layers	150 µm	100 µm	Minimum annular ring for the drill on outer signal layers
Annular Ring on Inner Layers	150 µm	100 µm	Minimum annular ring for the drill on inner signal layers
Accept missing Pads on Inner Layers	on	on	If active, missing copper pads on inner signal layers will not be reported
Distance to Copper	275 µm	275 µm	Minimum distance to surrounding copper on inner layers, if missing pads are accepted
Minimum Diameter	250 µm	200 µm	Minimum diameter of plated through holes
Minimum Drill Distance	300 µm	300 µm	Minimum Distance to any other Drill
<b>NPTH Rules</b>			
Mask Clearance for NPTHs	225 µm	200 µm	Minimum needed solder mask clearance for unplated through holes
Distance to Copper on Outer Layers	300 µm	300 µm	Minimum distance to surrounding copper on outer signal layers
Distance to Copper on Inner Layers	300 µm	300 µm	Minimum distance to surrounding copper on inner signal layers

# DFM – Preparations / Setup

DFM

Data Formats

Workflow

Preparations

Results

- Copper
- Mask
- Drills
- Components

## PCB Stack-Up Management

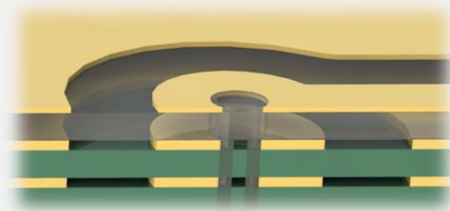
Layer

.position

.type (Component, Solder\_Mask, Signal, Drill, Rout)

.thickness

The stack-up definition can be done in the ECAD system or with PCB-Investigator. A library is used to share stack-ups. The Stack-Up can be imported / exported as XML, ODB++ and IPC2581



COMP_+_TOP	Component		
SPT	Solderpaste	0.00 µm	
SMT	UV-FLEX-HF	Soldermask	15.00 µm
1 SIGT	Copper;18	Signal	18.00 + 25.00 µm
Copper;18	18.00 µm	650 x 510 mm	18.00 µm
Copper;35	35.00 µm	650 x 510 mm	35.00 µm
Copper;70	70.00 µm	650 x 510 mm	70.00 µm
Copper;140	140.00 µm	650 x 510 mm	140.00 µm
Copper;400	400.00 µm	650 x 510 mm	400.00 µm
4 SIG4	Copper;35	Signal	35.00 µm
PREPREG_4	1080 [FZ 97]	Dielectric	102.00 µm
5 SIG5	Copper;35	Signal	35.00 µm
PREPREG_5	1080 [FZ 97]	Dielectric	102.00 µm
6 SIGB	Copper;18	Signal	18.00 + 25.00 µm
SMB	UV-FLEX-HF	Soldermask	15.00 µm
SPB	Solderpaste	0.00 µm	
DRILL	Drill		

# DFM – Preparations / Setup

DFM

Data Formats

Workflow

Preparations

Results

- Copper
- Mask
- Drills
- Components

**DRC violations have a strong impact on the quality and price**

Running the DRC helps to find violations and to categorize the design.

Before the DRC is started a pre-check reports the copper foil and smallest line used for each layer

Design Rule Check (Step: pcb)

Rule File: Standard Rule File Manager

Layer	Space (µm)	Trace (µm)	Type	Used Trace	Foil	Progress
<input checked="" type="checkbox"/> SMT	60	60	Mask Top			
<input checked="" type="checkbox"/> TOP	145	145	Signal Top	102 µm	18 µm	
<input checked="" type="checkbox"/> PWR	145	145	Signal Inner	152 µm	35 µm	
<input checked="" type="checkbox"/> LYR_1	145	145	Signal Inner	152 µm	35 µm	
<input checked="" type="checkbox"/> LYR_2	145	145	Signal Inner	152 µm	35 µm	
<input checked="" type="checkbox"/> GND	145	145	Signal Inner	152 µm	35 µm	
<input checked="" type="checkbox"/> BOTTOM	145	145	Signal Bot	101 µm	18 µm	
<input checked="" type="checkbox"/> SMB	60	60	Mask Bot			

☒ Scan for Opens/Shorts

Start

# DFM – Results

DFM

Data Formats

Workflow

Preparations

Results

- Copper
- Mask
- Drills
- Components

## DRC results for Bare Board and Assembly

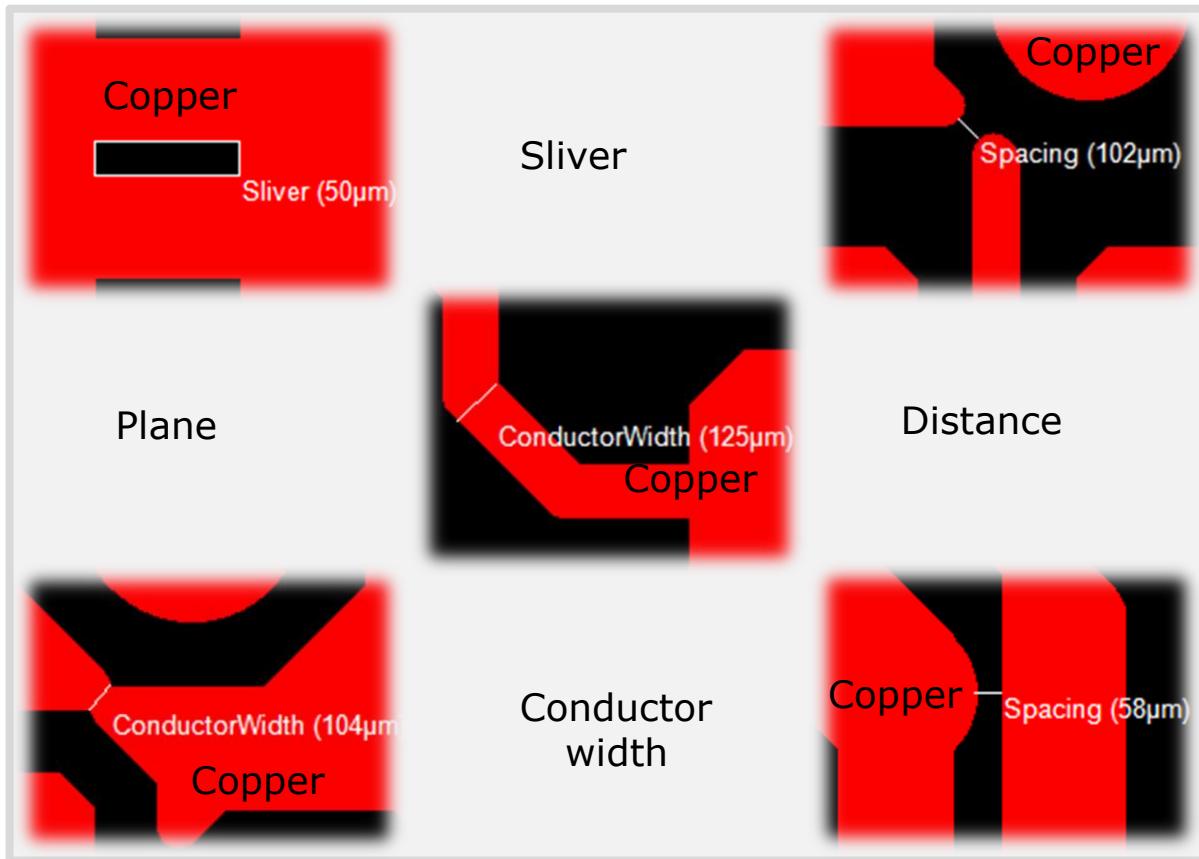
DRC for Solder Mask, Signals and Drills in conjunction to each other

All results are categorized and summed up per layer.

The screenshot shows the 'Bare Board DRC - Result Viewer: Standard\_2015.10.29\_145627' window. It features a 'Layers' list on the left with checkboxes for 'smt', 'sig1', 'sig2', 'sig3', 'sig4', 'sig5', 'sigb', 'smb', and 'drill'. The 'Error Types' list in the middle includes various categories like 'AcuteAngle', 'AnnularRingPTH', 'ConductorWidth', 'Coverage', 'ExposedCopper', 'MissingDrill', 'MissingMaskPTH', 'MissingMaskSMD', 'MissingMaskTP', 'MissingPad', 'NPTHtoCopper', 'Open', 'SameNetSpacing', 'Short', 'Sliver', 'Spacing', 'Stub', 'WrongMaskNPTH', 'WrongMaskPTH', 'WrongMaskPTHpad', 'WrongMaskSMD', and 'WrongMaskTP'. The 'Errors' list on the right displays specific error counts for each type, such as 'AcuteAngle (15)', 'AnnularRingPTH (2)', 'ConductorWidth (4)', 'Coverage (26)', 'ExposedCopper (12)', 'MissingDrill (1)', 'MissingMaskPTH (6)', 'MissingMaskSMD (14)', 'MissingMaskTP (1)', 'MissingPad (1)', 'NPTHtoCopper (1)', 'Open (269)', 'SameNetSpacing (2)', 'Short (619)', 'Sliver (2)', 'Spacing (5)', 'Stub (1)', 'WrongMaskNPTH (1)', 'WrongMaskPTH (1)', 'WrongMaskPTHpad (1)', 'WrongMaskSMD (21)', and 'WrongMaskTP (1)'. A 'Critical' column with checkboxes is also present. At the bottom, there is a checkbox for 'Show only critical Errors'.

# DFM – Copper Signal Check

## DRC Signal Analysis for outer and inner layers



# DFM – Solder Mask Check

## DRC Solder Mask Analysis

DFM

Data Formats

Workflow

Preparations

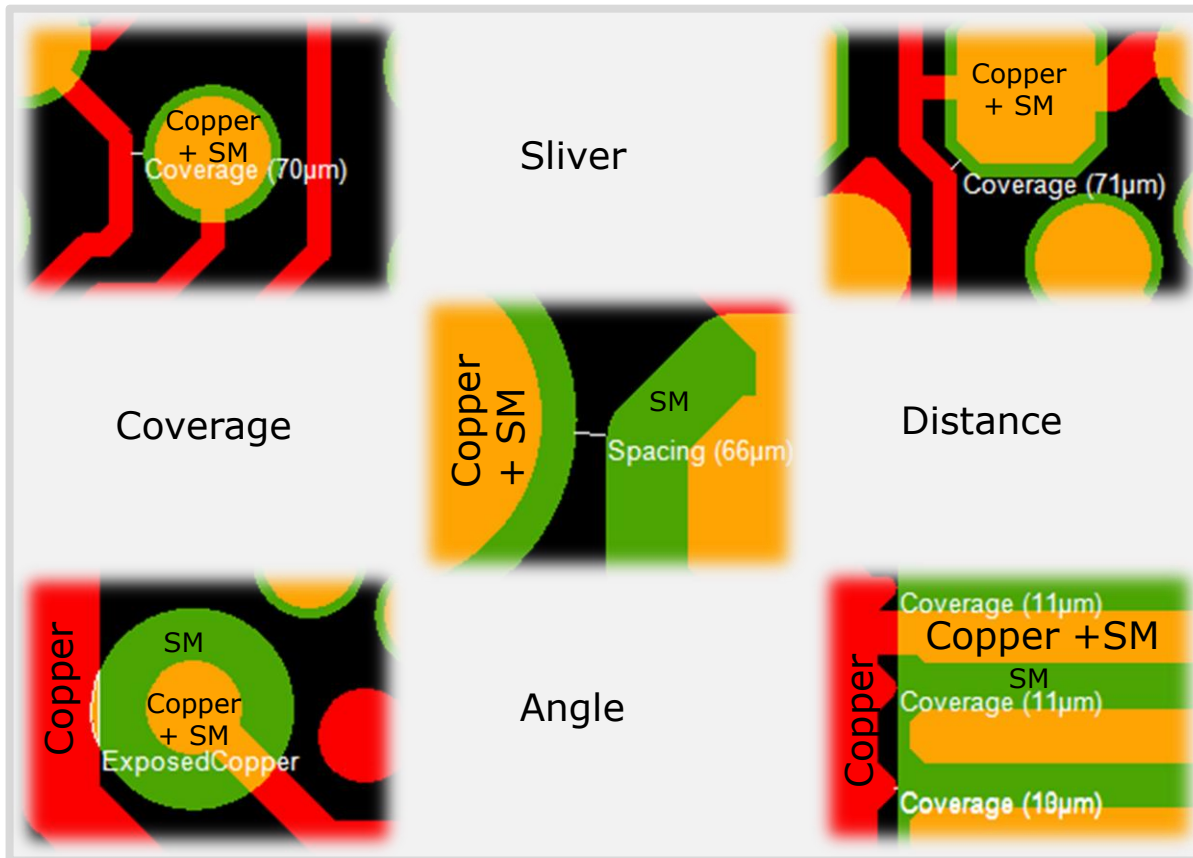
Results

- Copper

- **Mask**

- Drills

- Components

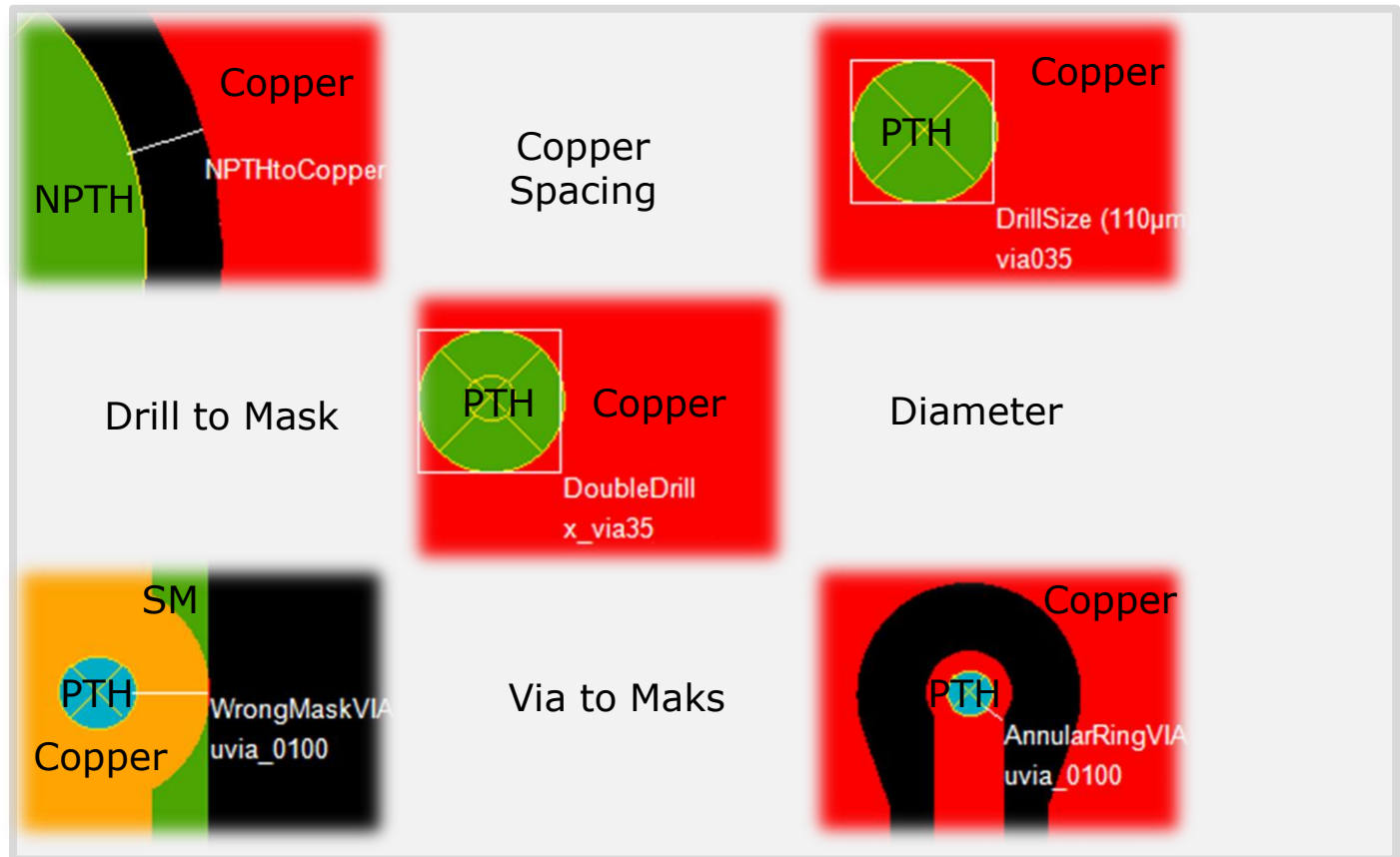




# DFM – Drill Check

## DRC Drill Analysis for mechanical and laser drills

DFM
Data Formats
Workflow
Preparations
Results
▪ Copper
▪ Mask
▪ <b>Drills</b>
▪ Components



# DFM – Component Check

DFM

Data Formats

Workflow

Preparations

Results

- Copper

- Mask

- Drills

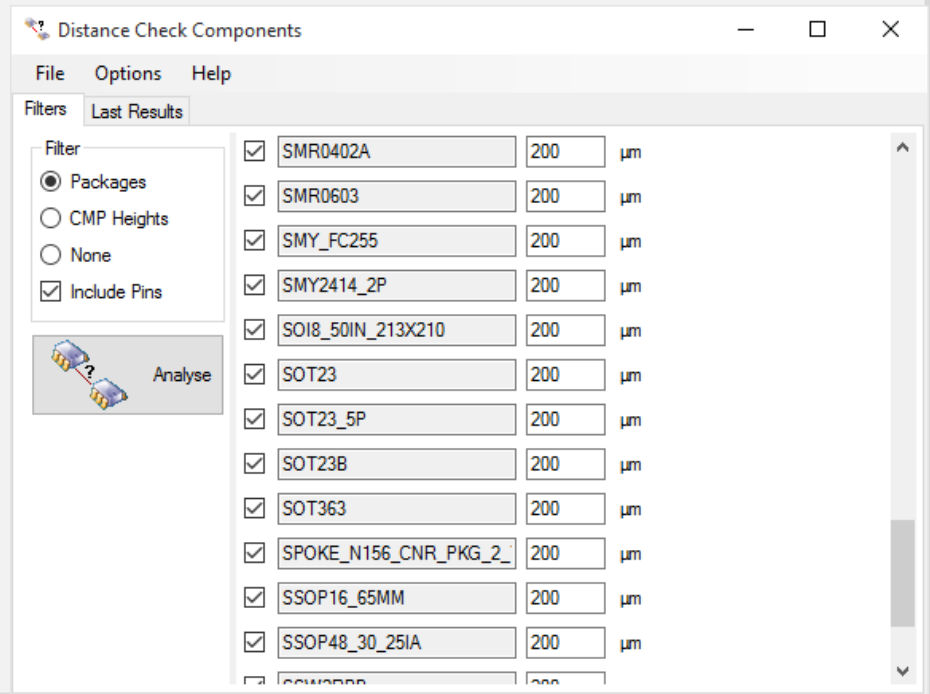
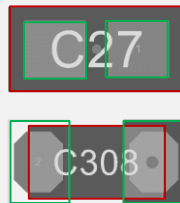
- Components

## Spacing between components to test manufacturing constraints

Set-up the rules to find AOI, Pick & Place and Test Point issues

Depending on the Component design in the library, the values have to be adjusted.

Component Body  
Component Pin



# DFM – Component Check

DFM

Data Formats

Workflow

Preparations

Results

▪ Copper

▪ Mask

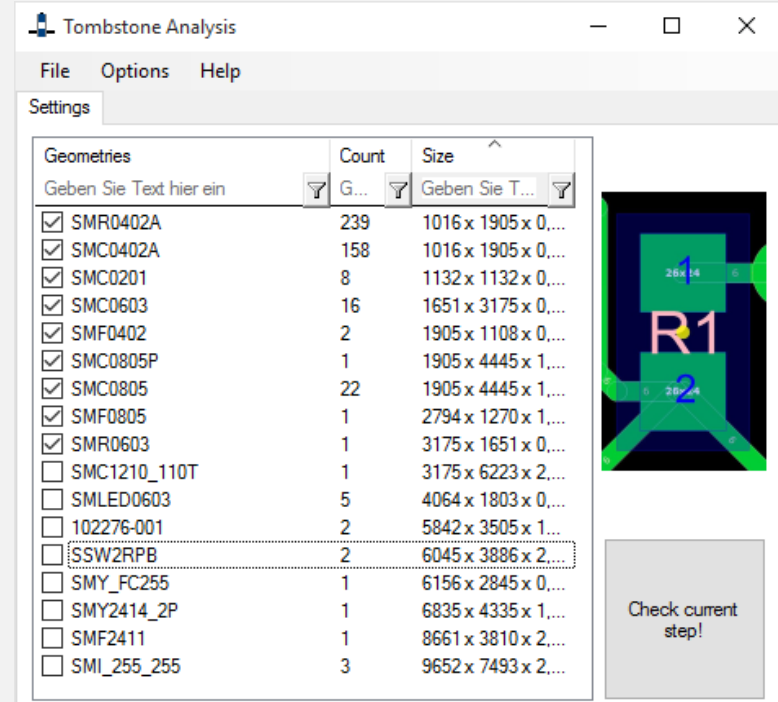
▪ Drills

▪ Components

**Tombstone effect during soldering, caused by different pin connection**

All 2 Pin components are checked for their signal connection

Possible hazard areas are small components with two pins. In cases where the difference from one pin connection to the other is too big, the component might be tipped upright during the soldering process.



Geometries	Count	Size
<input checked="" type="checkbox"/> SMR0402A	239	1016 x 1905 x 0,...
<input checked="" type="checkbox"/> SMC0402A	158	1016 x 1905 x 0,...
<input checked="" type="checkbox"/> SMC0201	8	1132 x 1132 x 0,...
<input checked="" type="checkbox"/> SMC0603	16	1651 x 3175 x 0,...
<input checked="" type="checkbox"/> SMF0402	2	1905 x 1108 x 0,...
<input checked="" type="checkbox"/> SMC0805P	1	1905 x 4445 x 1,...
<input checked="" type="checkbox"/> SMC0805	22	1905 x 4445 x 1,...
<input checked="" type="checkbox"/> SMF0805	1	2794 x 1270 x 1,...
<input checked="" type="checkbox"/> SMR0603	1	3175 x 1651 x 0,...
<input type="checkbox"/> SMC1210_110T	1	3175 x 6223 x 2,...
<input type="checkbox"/> SMLD0603	5	4064 x 1803 x 0,...
<input type="checkbox"/> 102276-001	2	5842 x 3505 x 1,...
<input type="checkbox"/> SSW2RPB	2	6045 x 3886 x 2,...
<input type="checkbox"/> SMY_FC255	1	6156 x 2845 x 0,...
<input type="checkbox"/> SMY2414_2P	1	6835 x 4335 x 1,...
<input type="checkbox"/> SMF2411	1	8661 x 3810 x 2,...
<input type="checkbox"/> SMI_255_255	3	9652 x 7493 x 2,...

# DFM – Component Check

DFM

Data Formats

Workflow

Preparations

Results

- Copper
- Mask
- Drills

▪ Components

## Stencil optimization to reduce pad lifting regarding IPC7525

### DRC for SMT soldering using a stencil

IPC Guidelines show how to define solder paste pads to ensure high quality during the process. To find Pads with a larger wall adhesive compared to the Pad surface, all Pads are calculated regarding the tested stencil thickness.

Get Paste Size Ratio

Layer	Ratio	Aspect Ratio	Area	Area Walls	X	Y	Width	Height	Stencil Thickness
Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text...	Geben Sie Text hier...
spb	0.64	2.75	0.03	0.04	26.45	-106.18	0.19	0.18	0.070
spb	0.64	2.18	0.03	0.04	26.45	-106.15	0.15	0.21	0.070
spb	0.64	2.75	0.03	0.04	26.45	-106.10	0.19	0.18	0.070
spb	0.64	2.75	0.03	0.04	26.49	-106.10	0.19	0.18	0.070
spb	0.64	2.18	0.03	0.04	26.53	-106.15	0.15	0.21	0.070
spb	0.64	2.75	0.03	0.04	26.49	-106.18	0.19	0.18	0.070
spt	0.72	3.31	0.04	0.05	81.64	-104.72	0.23	0.23	0.070
spb	0.72	3.31	0.04	0.05	81.64	-104.72	0.23	0.23	0.070
spt	0.74	4.17	0.04	0.05	-6.87	-98.01	0.29	0.15	0.070
spt	0.74	4.17	0.04	0.05	14.47	-111.98	0.29	0.15	0.070
spt	0.74	4.17	0.04	0.05	15.23	-105.24	0.29	0.15	0.070
ent	0.74	4.17	0.04	0.05	16.89	-106.85	0.29	0.15	0.070

Stencil thickness: 70 µm

Mark lines with ratio < 0.66

☐ Check only in PCB Profile

Calculate

CSV Export Close

# Software Portfolio

PCB-Investigator

[www.pcb-investigator.com](http://www.pcb-investigator.com)

Native Board Import (3D Interface to CATIA, SiemensNX, SolidWorks, SolidEdge)

[www.sts-development.biz](http://www.sts-development.biz)

GerberLogix

[www.GerberLogix.com](http://www.GerberLogix.com)

Online Gerber Viewer

[www.Gerber-Viewer.com](http://www.Gerber-Viewer.com)

Software Development, CAD Converter, data connection

[www.easyLogix.de](http://www.easyLogix.de)

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