

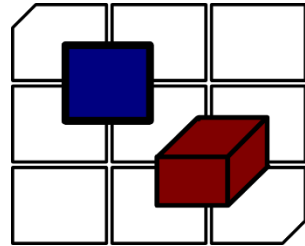
# EASYLOGIX.DE



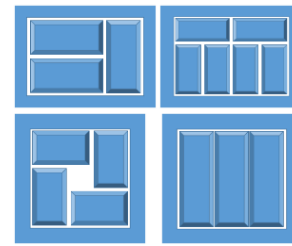
PCB-Investigator



PCB-I-Online



Native Board Import



Panel Optimizer



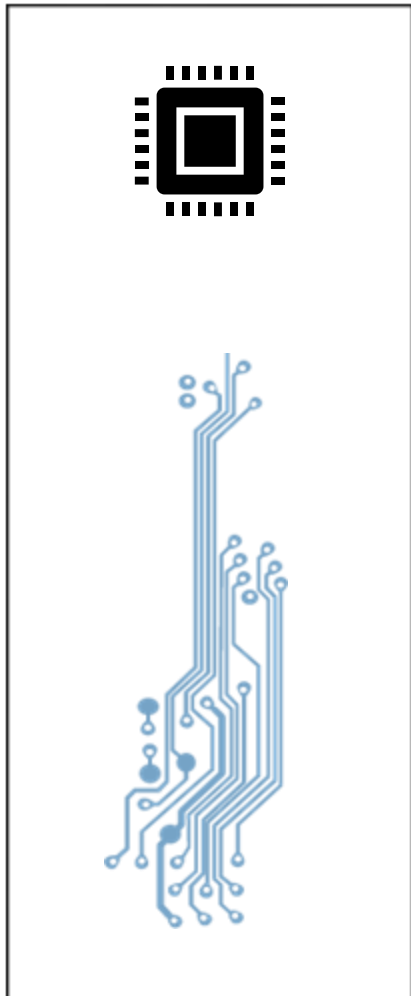
PCB-I-Physics



PLM

## High Quality Stencil Preparation

# Product Categories



PCB Assembly	PCB Manufacturing	PCB Testing
Material Libraries	Component Libraries	Package Libraries
EMS Manufacturing	Layout Design	Thermal & Current Simulation
Digital Twin	Design Review	Equipment Integration •AOI, Solder Machine, Boundary Scan, Direct Imaging

# Advanced Stencil Preparation

## Increase in Efficiency and Productivity

PCB-Investigator automates data preparation while allowing the flexibility customers needs.  
Takin care of all different types of stencils and components.

## Standard Stencil design / Step-Stencil Technologies

Train your CAD System for best results  
Use knowledge getting from components  
Adding the experience from internal production  
Set up a looped process to learn with each product

## **IPC-7525A**

Stencil Design Guidelines

- **Electroforming**
- **Laser Cutting**
- **Chemical Etching**
  
- **Stainless Steel SMT Stencils**
- **Mylar and Kapton SMT Stencils**

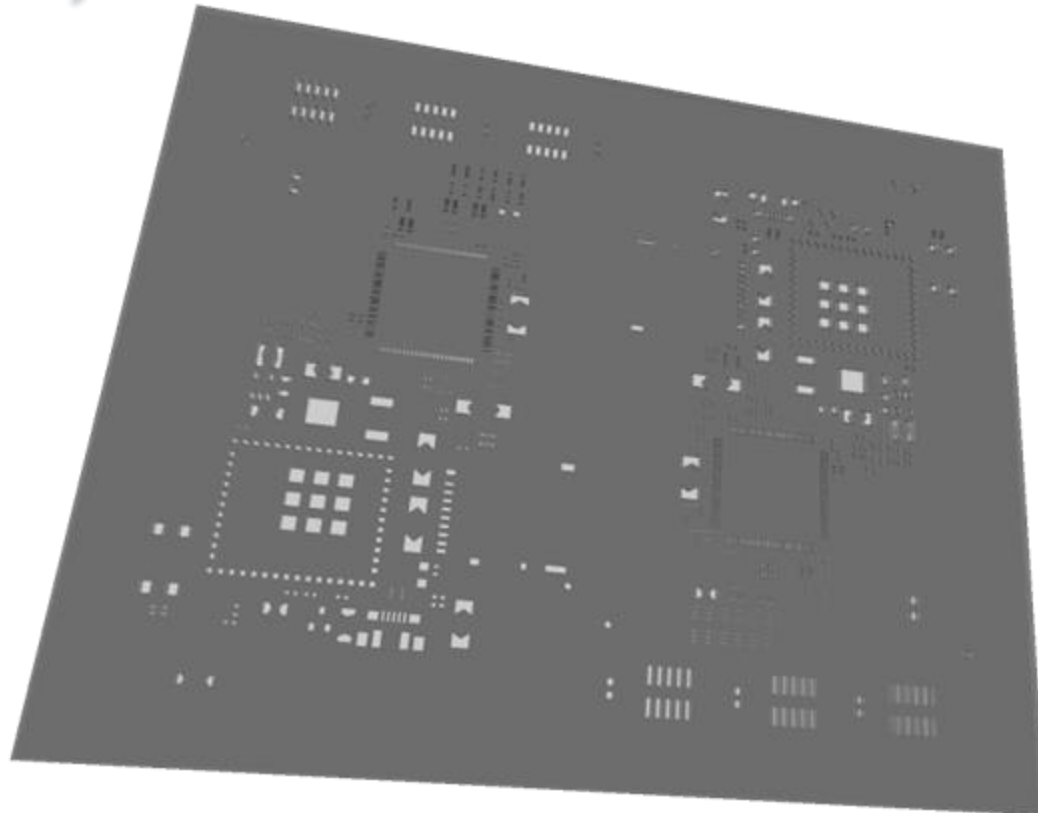
# Advanced Stencil Preparation

One of the features of PCB-Investigator is its ability to handle all different types of stencils and components. This includes standard stencil design and step-stencil technologies, as well as stencils made using electroforming, laser cutting, chemical etching, and other techniques. PCB-Investigator can also support different types of stencil materials.

In addition to its automation capabilities, PCB-Investigator also offers flexibility to meet the specific needs of customers. This includes the ability to train the CAD system for optimal results, use knowledge gained from components and internal production experience, and set up a looped process to learn with each product. By using PCB-Investigator, customers can streamline their data preparation process and improve their efficiency and productivity in PCB manufacturing.

# Advanced Stencil Preparation

Area Editor  
Stencil Generator  
Stencil Analysis



Suitable for both standard and STEP stencils.

Switching from predefined to rule-based creation improves the automation process, making it more reliable and independent.

This approach also puts the production technology in the forefront, ensuring that the process is tailored to the specific requirements of the application..

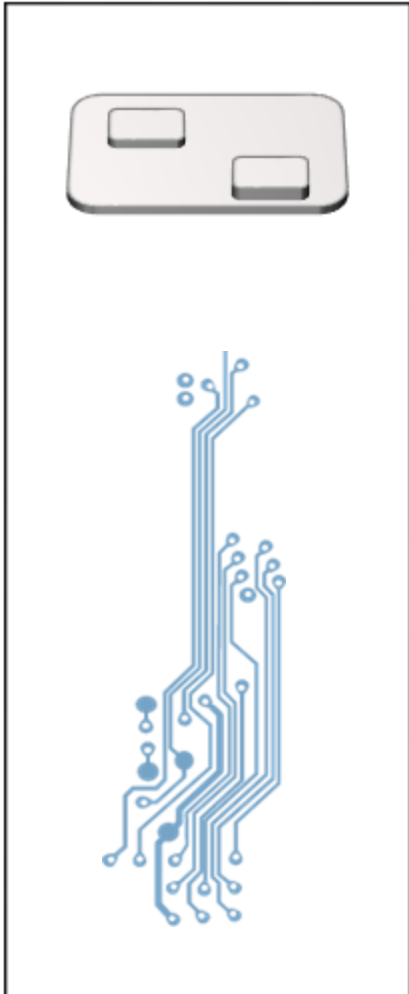
# Package Types

Assign the right optimization to each package

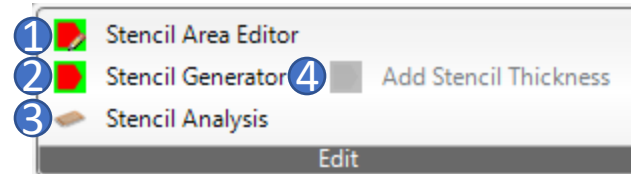
- QFN - quad flat pack
- PQFN - power quad flat-pack, no-leads, with exposed die-pad[s] for heat sinking.
- BGA - ball grid array
- CGA - column grid array
- CCGA - ceramic column grid array
- BGA - micro-BGA, with ball spacing less than 1mm.
- COB - chip-on-board
- COF - chip-on-flex
- COG - chip-on-glass
- SOIC Small outline integrated circuit
- SOP Small outline package
- PLCC Plastic leaded chip carrier
- TSOP Thin small outline package
- SSOP Shrink small outline package
- TSSOP Thin shrink small outline package
- QSOP Quarter-size small outline package
- VSOP Very small outline package
- LQFP Low profile quad flat pack
- PQFP Plastic quad flat pack
- CQFP Ceramic quad flat pack
- TQFP Thin quad flat pack
- MLP – Lead-frame package
- MQFP - Metric Quad Flat Pack
- CSP – Chip Scale Package

Using PCB-Investigator, customers can automate the stencil preparation process and streamline their PCB manufacturing workflow. The tool can help to ensure that the correct stencils are created for the package types being used, improving efficiency and reducing the risk of errors.

# Stencil Wizard



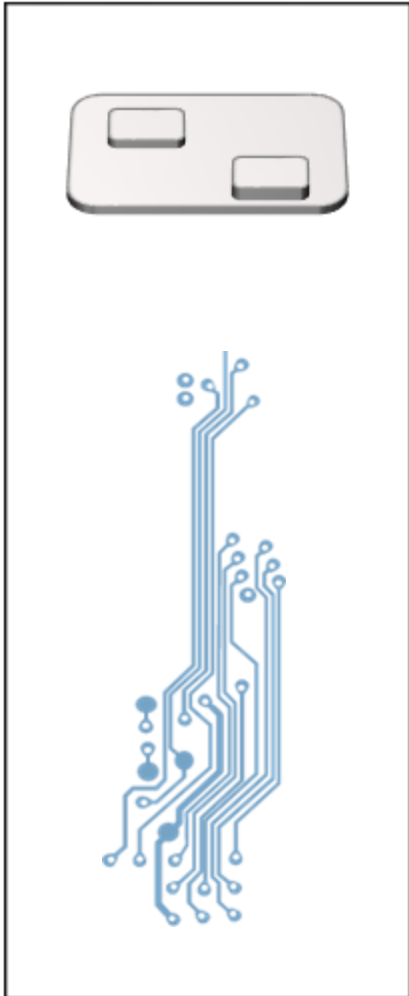
**Advanced rule-based stencil generation taking component information into account**



To create high-quality SMT pads for your stencil, the following steps should be taken:

- Create all necessary patchwork and steps for your stencil
- Use all relevant rules to create the SMT pads
- Ensure that the stencil conforms to IPC standards
- Set the overall thickness of the stencil to the appropriate level for the specific application.

# Stencil Wizard



## **Advanced rule-based stencil generation taking component information into account**

PCB-Investigator is used to create patch work and steps for stencils. PCBI can be configured to use a variety of rules to create high quality SMT pads, ensuring that the stencils produced meet industry standards and are suitable for use in PCB manufacturing.

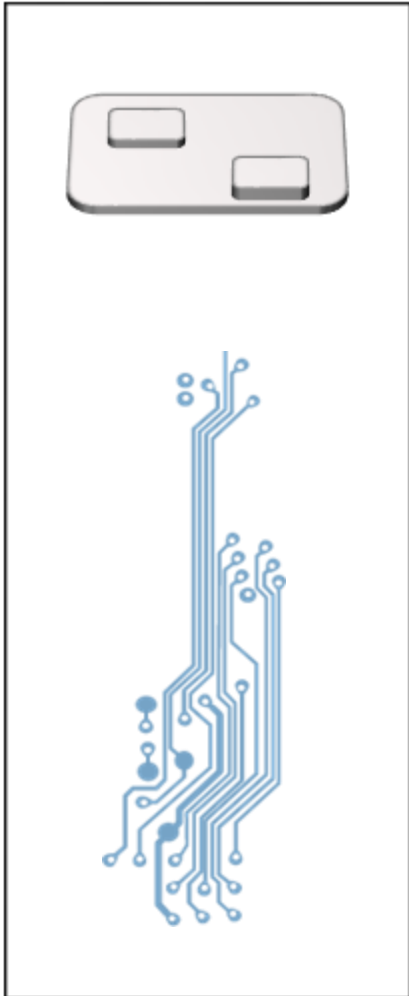
In addition to creating the patch work and steps, PCB-Investigator can also be used to check the stencil against IPC (International Electrotechnical Commission) standards.

This can ensure that the stencil meets the necessary quality and performance requirements for your project.

PCB-Investigator can set the overall thickness of the stencil, ensuring that it is suitable for use with the particular manufacturing process and equipment being used. By using PCB-Investigator, customers can streamline their stencil preparation process and improve the efficiency and quality of their PCB manufacturing operations.



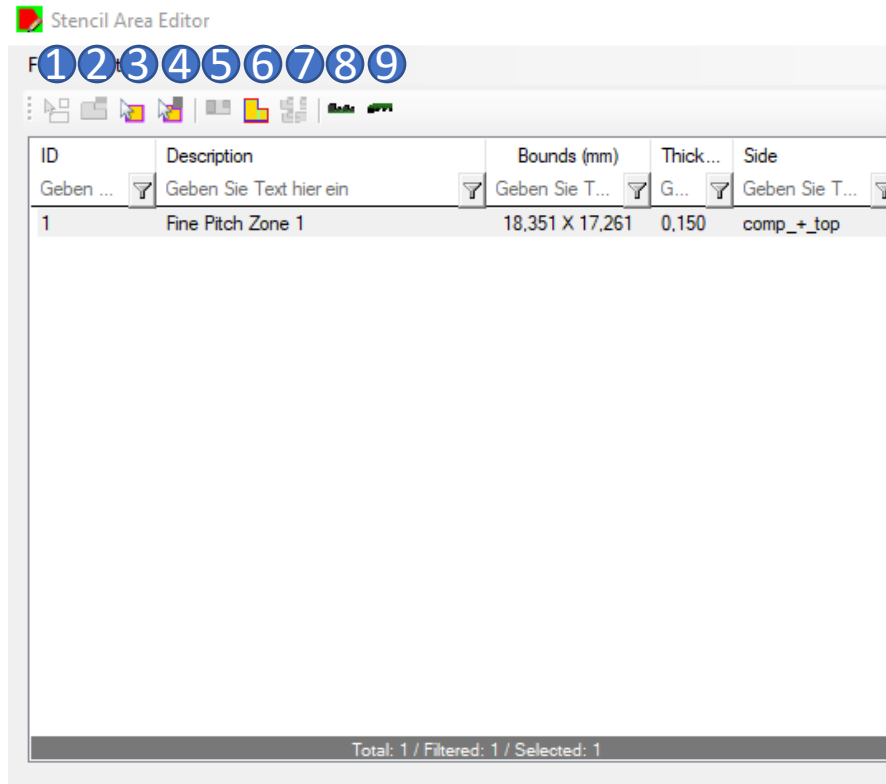
# Stencil Wizard



## Stencil Area Editor operations

Stencil Area Editor

F 1 2 3 4 5 6 7 8 9

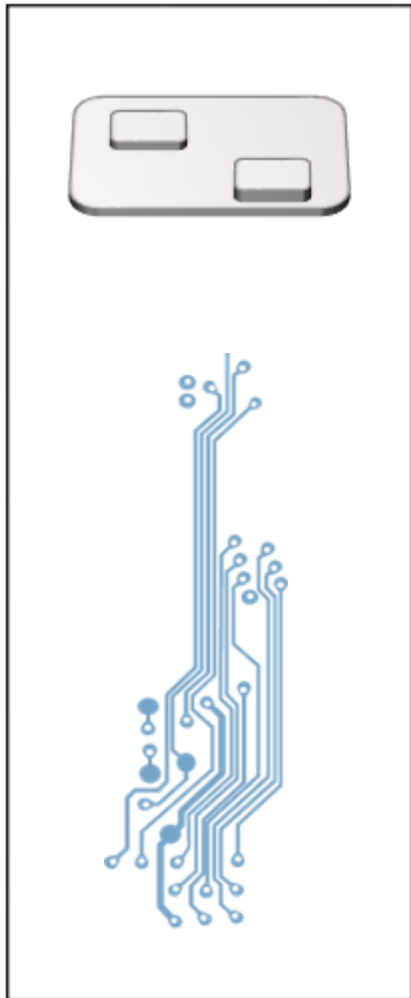


ID	Description	Bounds (mm)	Thick...	Side
1	Fine Pitch Zone 1	18,351 X 17,261	0,150	comp_+_top

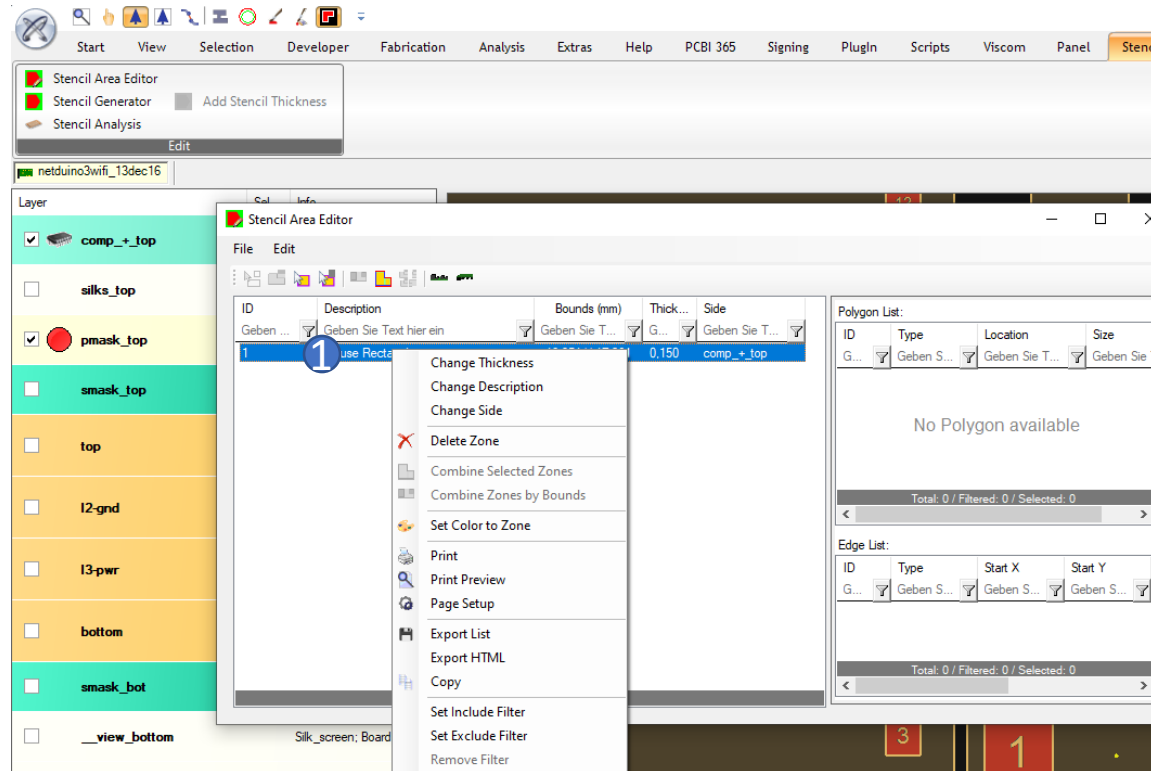
Total: 1 / Filtered: 1 / Selected: 1

1. Add selection as zone
2. Set Area
3. Add zone by rectangle
4. Add zone by rectangle with cutouts
5. Combine selection
6. Add zone rectangle
7. Combine zones overlapping
8. Switch to Top View
9. Switch to Bot View

# Stencil Area Editor



## Edit base settings for each area



Stencil Area Editor

File Edit

ID	Description	Bounds (mm)	Thick...	Side
1	use Rect...		0.150	comp_+_top

Polygon List:

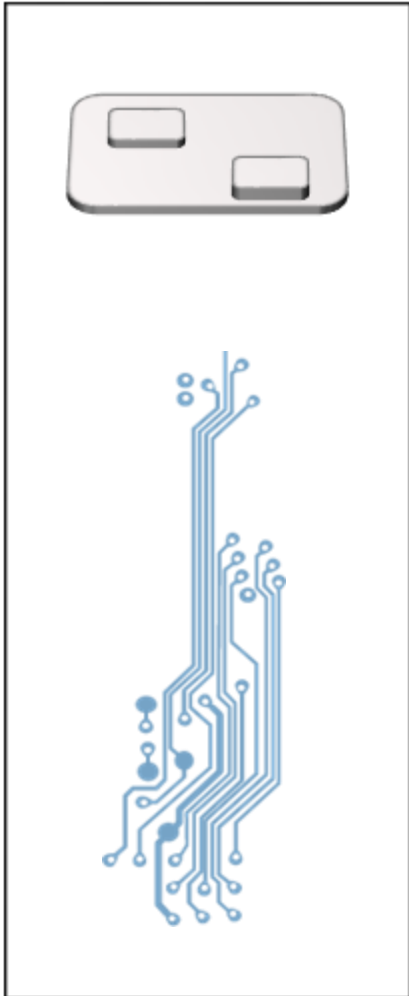
ID	Type	Location	Size
G...	Geben S...	Geben Sie T...	Geben Sie

Edge List:

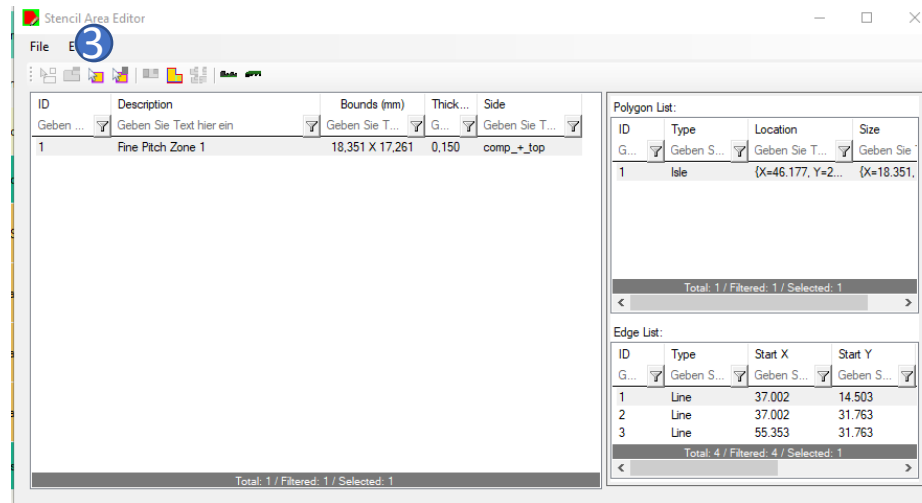
ID	Type	Start X	Start Y
G...	Geben S...	Geben S...	Geben S...

## 1. Context menu

# Stencil Area Editor

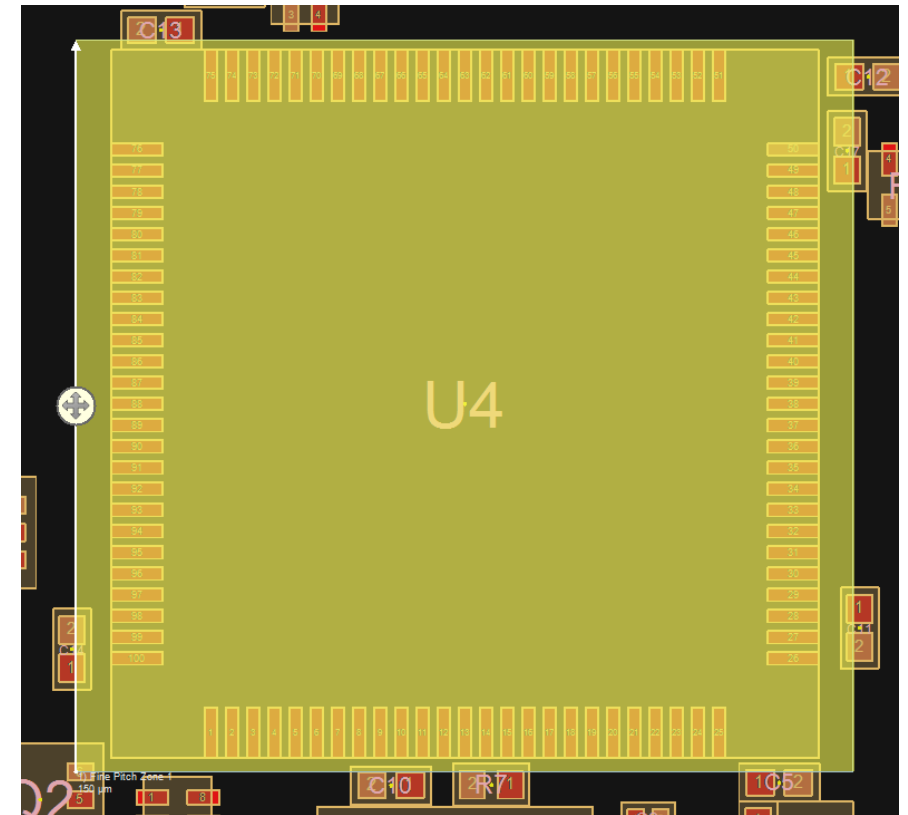


## Edit the shape

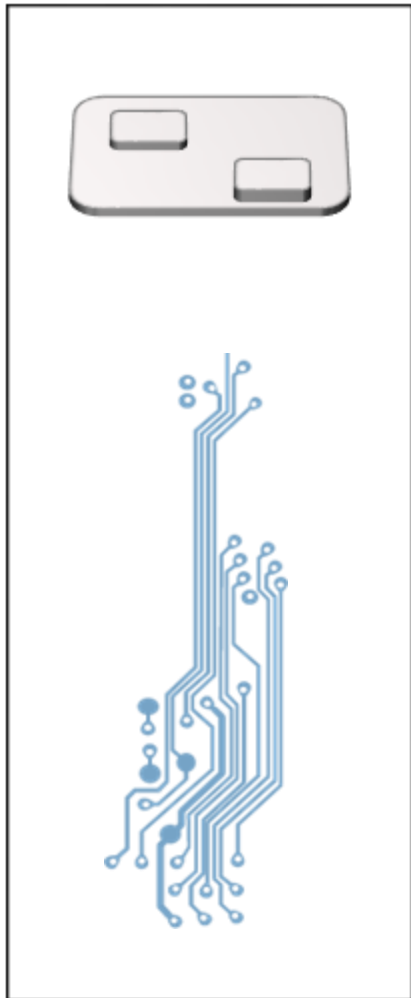


### 3. Add a new zone by drawing a rectangle

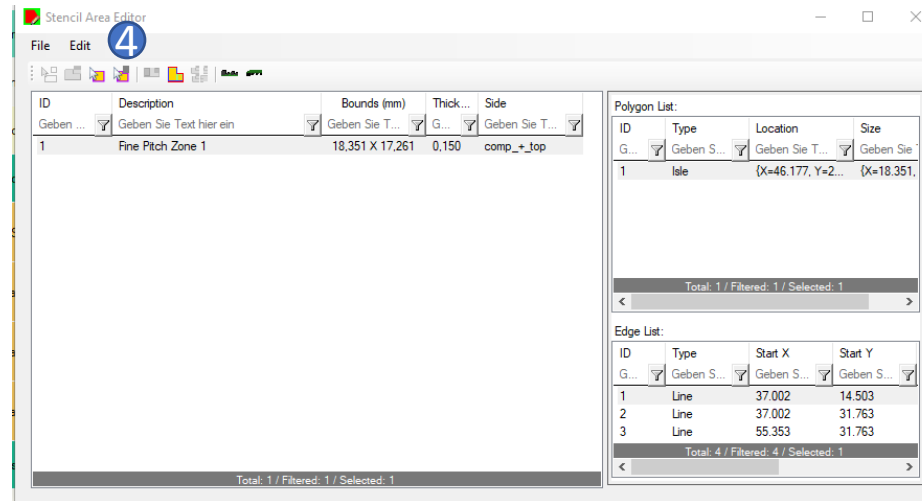
Note: For high quality, it is recommended not to cut pin pads. You can combine areas e.g. from different parts to get ideal areas.



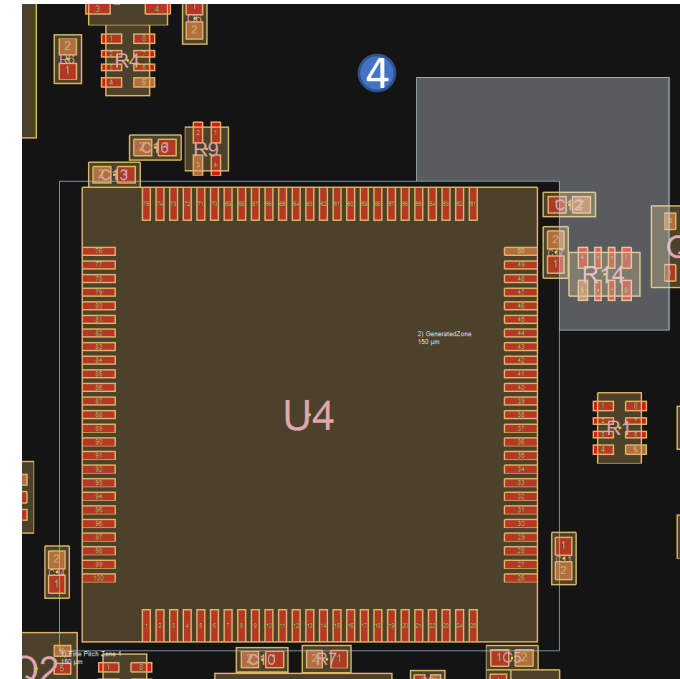
# Stencil Area Editor



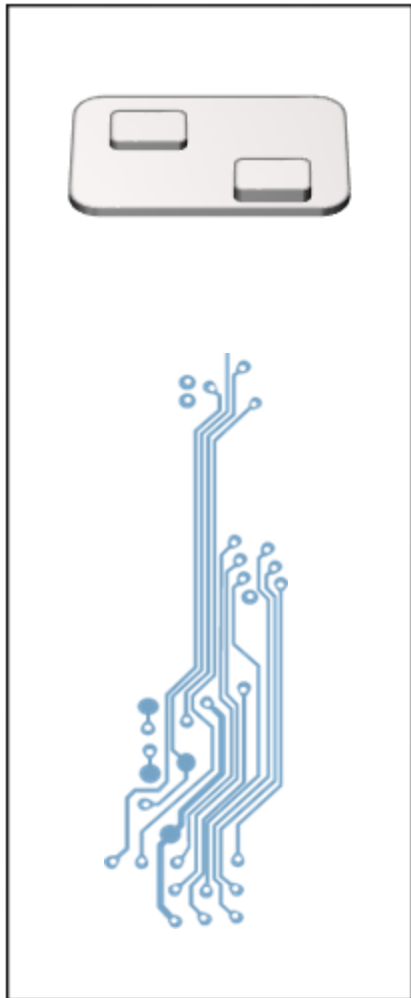
## Zone function



4. Add a new zone with cutting out a previous zone by drawing a rectangle



# Stencil Area Editor



## Zone function

Stencil Area Editor

File Edit

ID	Description	Bounds (mm)	Thick...	Side
1	Combination: Fine Pitch Zone 1, Gen...	22,382 X 21,076	0,150	comp_+_top
2	GeneratedZone	16,700 X 16,700	0,150	comp_+_top

Polygon List:

ID	Type	Location	Size
G...	Geben S...	Geben Sie T...	Geben Sie

No Polygon available

Total: 0 / Filtered: 0 / Selected: 0

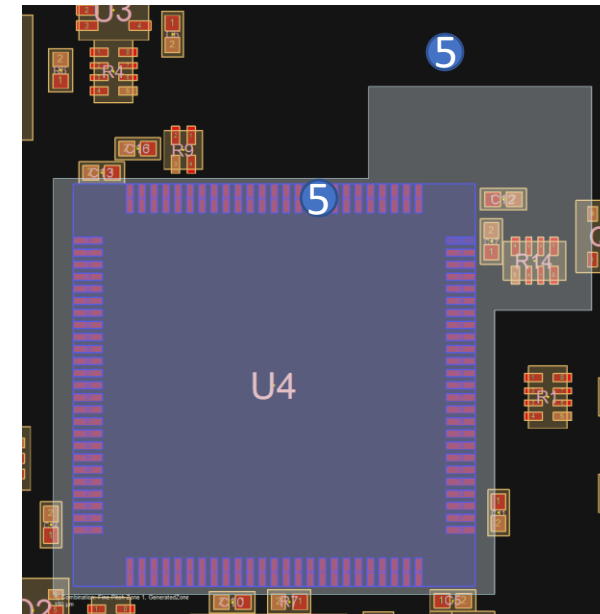
Edge List:

ID	Type	Start X	Start Y
G...	Geben S...	Geben S...	Geben S...

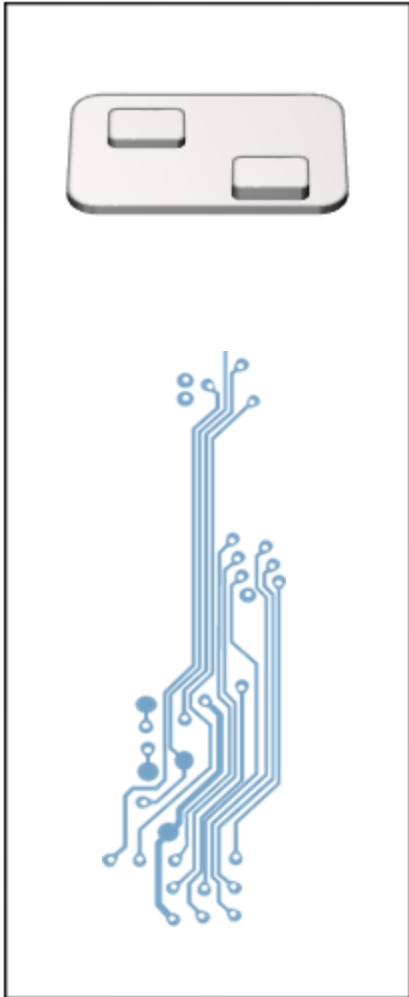
Total: 0 / Filtered: 0 / Selected: 0

Total: 2 / Filtered: 2 / Selected: 2

5. Combine different zones to one zone



# Stencil Wizard



## Clearance analysis

PCB-Investigator / www

Start View Selection Developer Fabrication Analysis Extras Help PCB1 365 Signing Plugin Scripts Viscom Panel Stencil

Stencil Area Editor  
 Stencil Generator Add Stencil Thickness  
 Stencil Analysis  
 Edit

netduino3wifi\_13dec16

Layer Sel. Info

- comp\_+\_top Obj:94; Co...
- silks\_top Silk\_scre...
- pmask\_top Obj:476; S...
- smask\_top Obj:525; S...
- top Obj:2984; S...
- I2-grnd Signal; Boa...
- I3-pwr Signal; Boa...
- bottom Signal; Boa...
- smask\_bot Solder\_ma...
- \_\_view\_bottom Silk\_screen; Board
- silks\_bot Silk\_screen; Board

Stencil Area Editor

File Edit

Stencil Distance Rule

ID	Description	Bounds (mm)	Thick...	Side
1	Combination: Fine Pitch Zone 1, Gen...	22.382 X 21.076	0,150	comp_+_top
2	GeneratedZone	16,700 X 16,700	0,150	comp_+_top

Polygon List:

ID	Type	Location	Size
G...	Geben S...	Geben Sie T...	Geben Sie

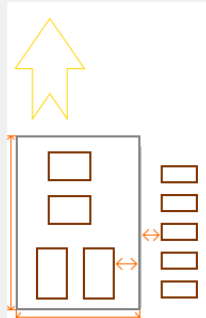
No Polygon available

Zone Distance Definitions

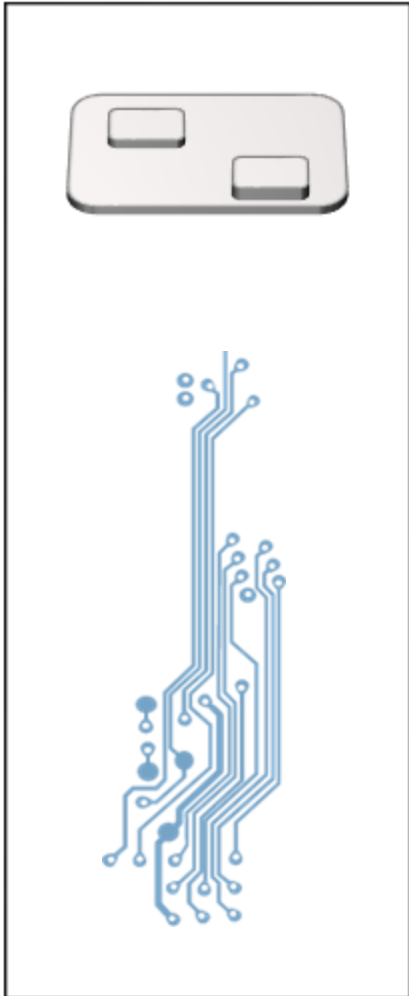
	Step Width Minimum (MM)	Step Height Minimum (MM)	Pad Distance Minimum Both Directions (MM)	IPCmm	Distance of zone to zone heights (MM)	Rakel Type
	0,25	0,25	0,3	0,36	0,01	Standardrakel (n...
1	1	1	0,9	1,08	0,03	Standardrakel (n...
10	2	1,7	1,7	1,8	0,05	Standardrakel (n...
30	10	5,8	5,8	3,6	0,1	Standardrakel (n...
75	10	12,0000000000000...	9	0,25	0,25	Standardrakel (n...
10	1	1,600000000000000...	1,8	0,05	Standardrakel (d...	
20	5	3,8	3,6	0,1	Standardrakel (d...	
30	10	11,3	9	0,25	Standardrakel (d...	
0,25	0,25	0,3	0,36	0,01	Gedünnte Rakel ...	
1,5	1,5	0,6	1,08	0,03	Gedünnte Rakel ...	
10	1,5	1,500000000000000...	1,8	0,05	Gedünnte Rakel ...	
10	1,5	2,5	3,6	0,1	Gedünnte Rakel ...	
30	10	9	9	0,25	Gedünnte Rakel ...	

Rakel Direction  
 Bottom Top  Left Right

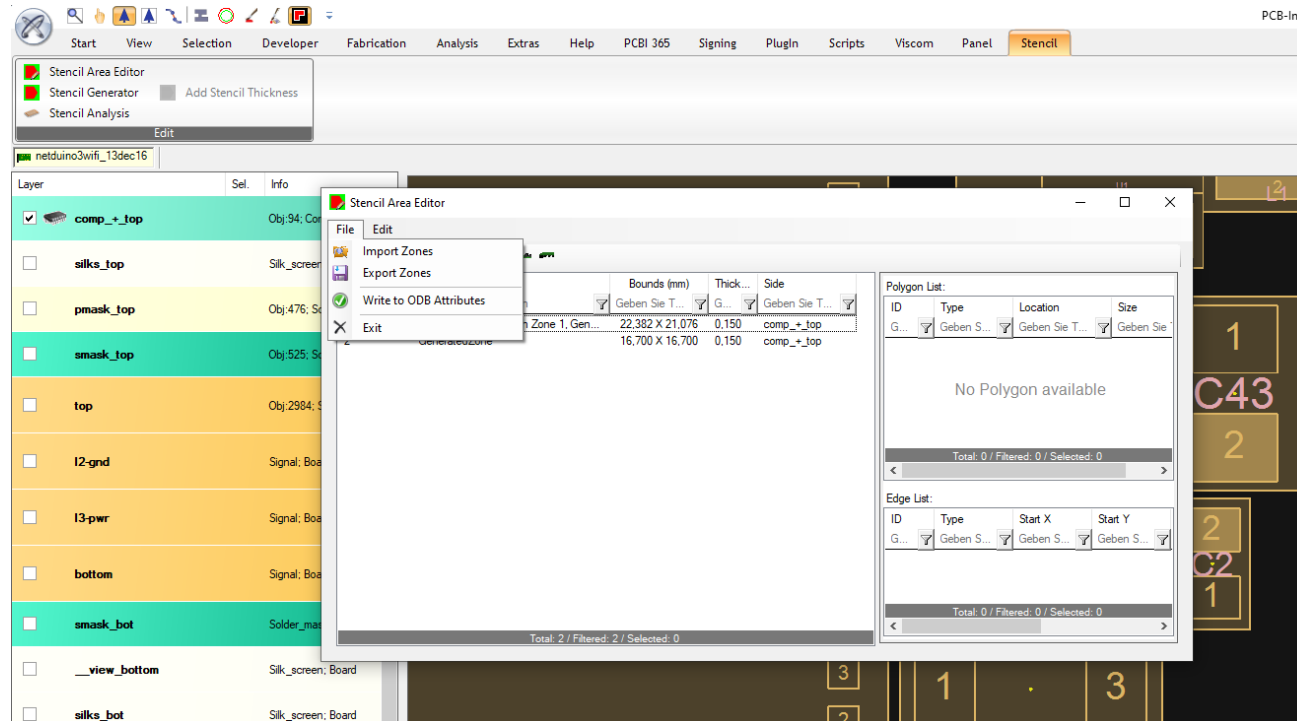
OK



# Stencil Area Editor



## Manage zone settings



netduino3wifi\_13dec16

Layer

Layer	Sel.	Info
<input checked="" type="checkbox"/> comp_+_top		Obj:94; Co...
<input type="checkbox"/> silks_top		Silk_scre...
<input type="checkbox"/> pmask_top		Obj:476; S...
<input type="checkbox"/> smask_top		Obj:525; S...
<input type="checkbox"/> top		Obj:2984; S...
<input type="checkbox"/> I2-gnd		Signal; Bo...
<input type="checkbox"/> I3-pwr		Signal; Bo...
<input type="checkbox"/> bottom		Signal; Bo...
<input type="checkbox"/> smask_bot		Solder_mas...
<input type="checkbox"/> __view_bottom		Silk_screen; Board
<input type="checkbox"/> silks_bot		Silk_screen; Board

Stencil Area Editor

File Edit

- Import Zones
- Export Zones
- Write to ODB Attributes
- Exit

Zone 1, Gen...	Bounds (mm)	Thick...	Side
	Geben Sie T...	G...	Geben Sie T...
	22.382 X 21.076	0.150	comp_+_top
	16.700 X 16.700	0.150	comp_+_top

Polygon List:

ID	Type	Location	Size
G...	Geben S...	Geben Sie T...	Geben Sie

No Polygon available

Total: 0 / Filtered: 0 / Selected: 0

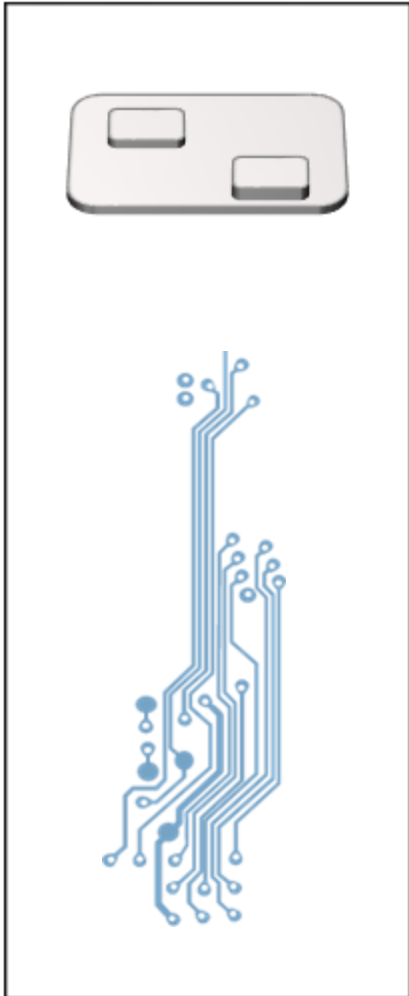
Edge List:

ID	Type	Start X	Start Y
G...	Geben S...	Geben S...	Geben S...

Total: 0 / Filtered: 0 / Selected: 0

Zone settings can be saved in ODB attributes, exported as xml and imported from xml.

# Stencil Area Editor

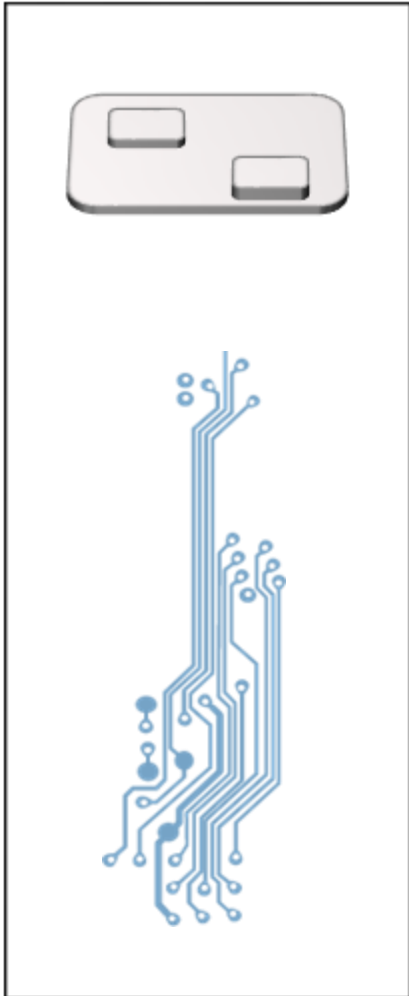


## Add zones by predefined drawings

1. Increased flexibility: A step stencil allows for different paste deposition levels in different areas, which can be useful for specific applications.
2. Improved accuracy: The different thickness levels in a step stencil can provide more precise and accurate paste transfer, as the aperture walls are closer to the pads in some areas.
3. Reduced paste bridging: The different thickness levels in a step stencil can reduce the risk of paste bridging between apertures, which can lead to better yields and improved overall quality of the soldered joints.
4. Reduced costs: A step stencil allows for more efficient use of paste, which can lead to reduced costs for the soldering process.
5. Increased process control: By adjusting the thickness of the stencil at different areas, it allows better control of the paste depositon, which can have a positive impact on the final product quality.



# Stencil Area Editor



## Add zones by predefined drawings

Stencil Area Editor

1 Edit

ID	Description	Bounds (mm)	Thick...	Side
1	Combination: Fine Pitch Zone 1, Gen...	22,382 X 21,076	0,150	comp_+_top
2	GeneratedZone	16,700 X 16,700	0,150	comp_+_top

Polygon List:

ID	Type	Location	Size
G...	Geben S...	Geben Sie T...	Geben Sie

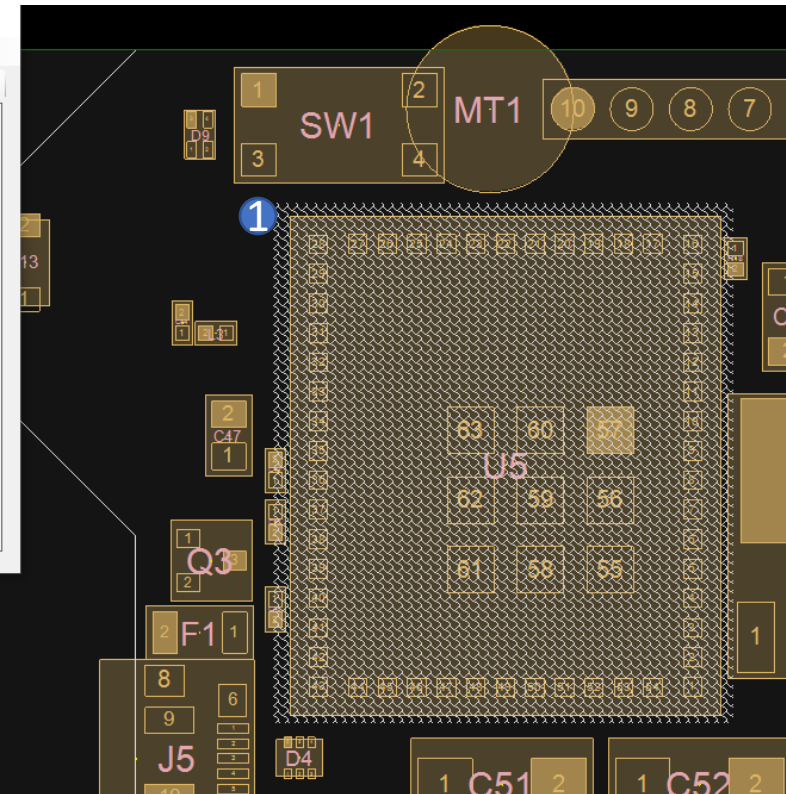
No Polygon available

Total: 0 / Filtered: 0 / Selected: 0

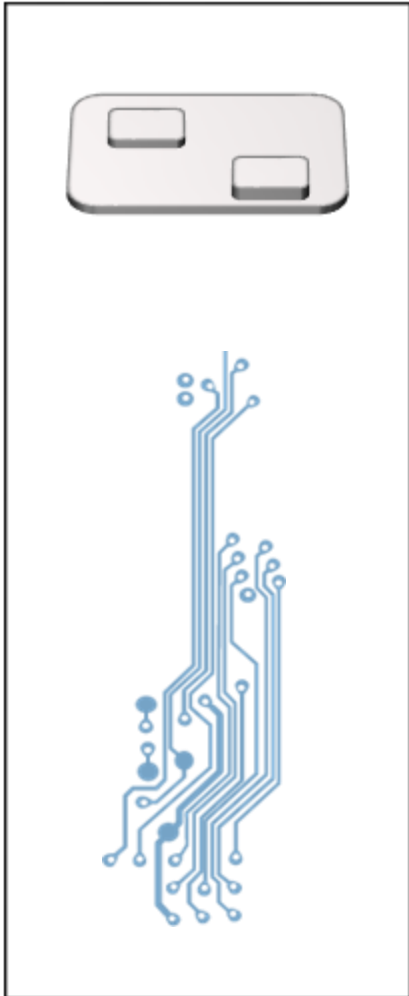
Edge List:

ID	Type	Start X	Start Y
G...	Geben S...	Geben S...	Geben S...

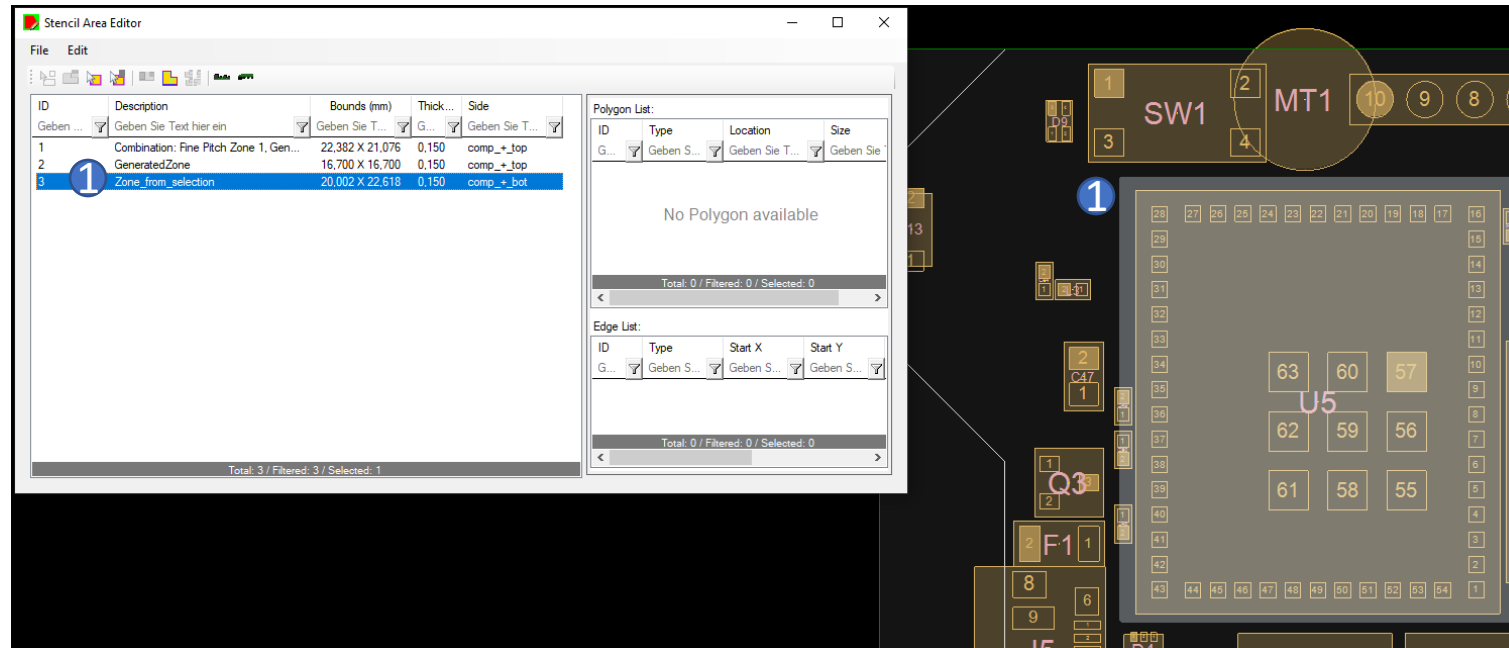
Total: 0 / Filtered: 0 / Selected: 0



# Stencil Area Editor



## Add zones by predefined drawings



The screenshot shows the 'Stencil Area Editor' window with a table of zones and a PCB layout in the background. The table lists three zones:

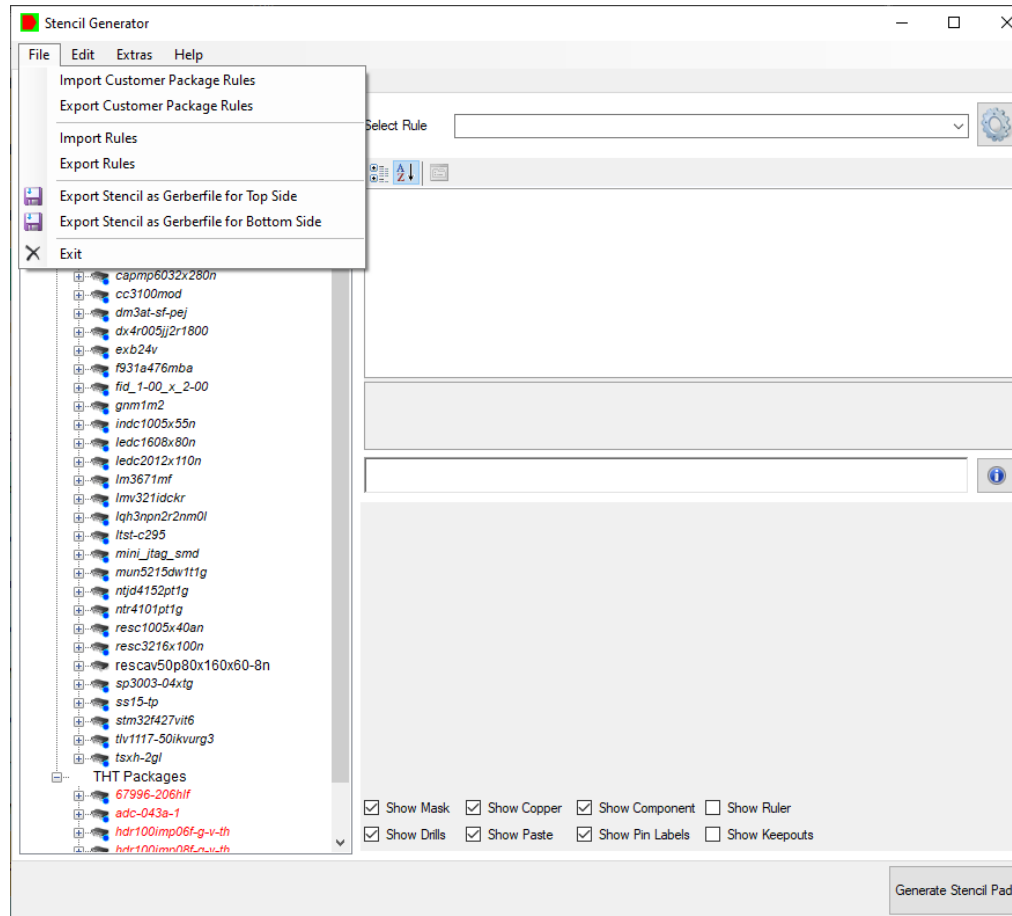
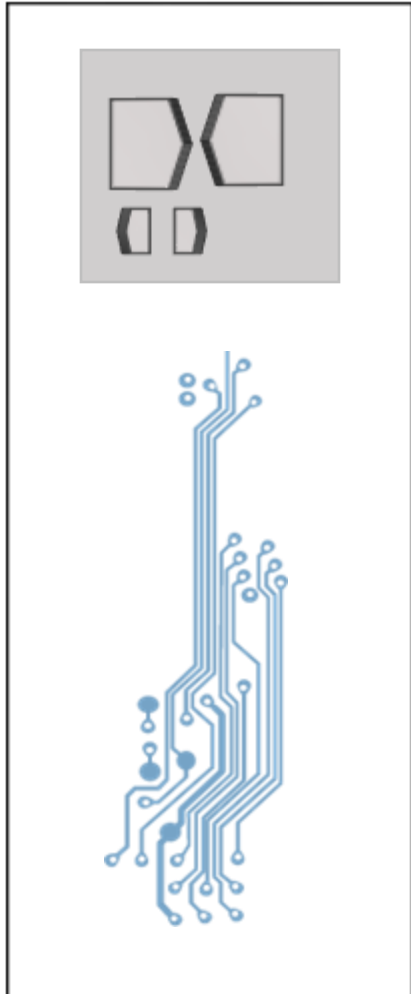
ID	Description	Bounds (mm)	Thick...	Side
1	Combination: Fine Pitch Zone 1, Gen...	22.382 X 21.076	0.150	comp_+_top
2	GeneratedZone	16.700 X 16.700	0.150	comp_+_top
3	Zone_from_selection	20.002 X 22.618	0.150	comp_+_bot

The PCB layout in the background shows various components labeled with IDs like SW1, MT1, U5, Q3, F1, C47, and D4, along with a grid of numbered pads.

- Improved accuracy: Smaller thickness stencils can provide more precise and accurate paste transfer, as the aperture walls are closer to the pads.
- Better paste release: The thinner stencils can lead to better release of the paste from the apertures, resulting in more consistent and reliable paste deposition.
- Reduced paste bridging: Thinner stencils can reduce the risk of paste bridging between apertures, which can lead to better yields and improved overall quality of the soldered joints.
- Reduced costs: Thin stencils require less material, which can lead to reduced manufacturing costs.
- Increased flexibility: Thin stencils can be more flexible, which can be useful in applications where the stencil needs to conform to irregular or curved surfaces.

# Stencil Generator

## Main setup for paste pad creation



The Stencil Generator uses all zones defined by the Stencil Area Editor. If there are no zones the outline will be used as main zone.

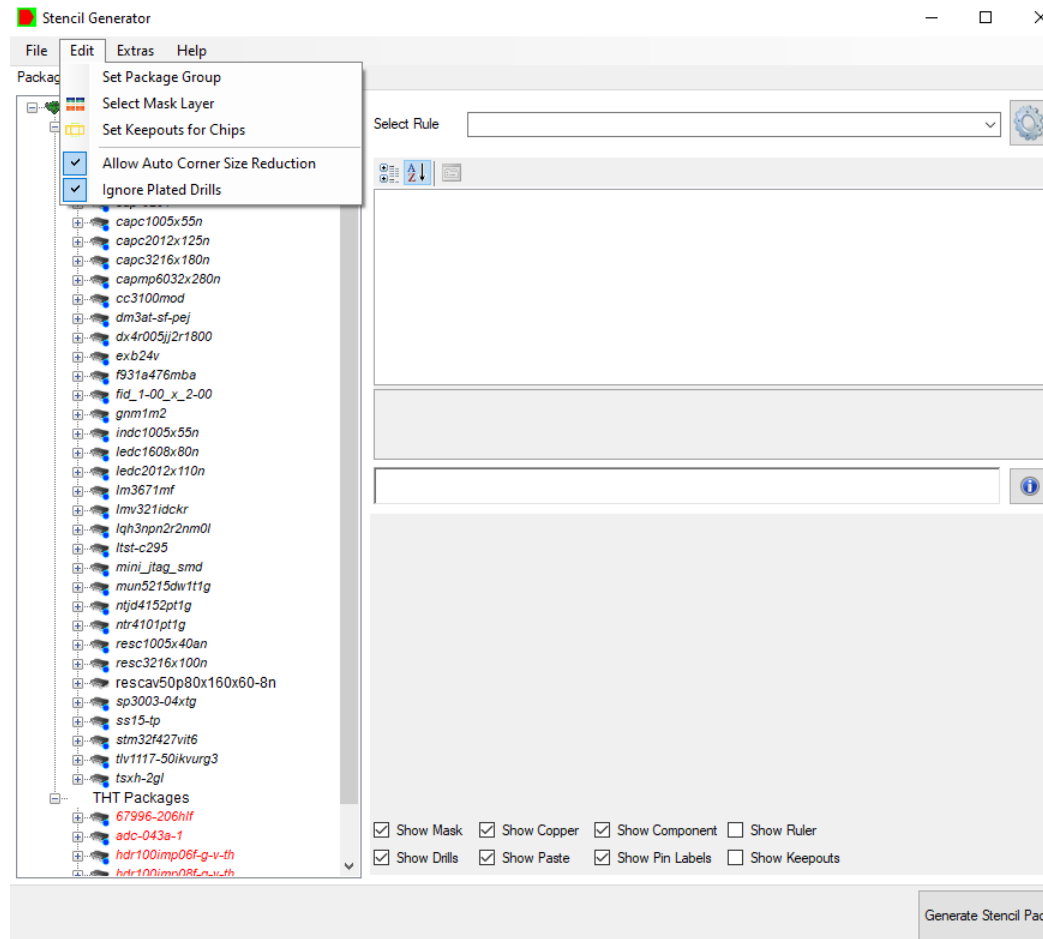
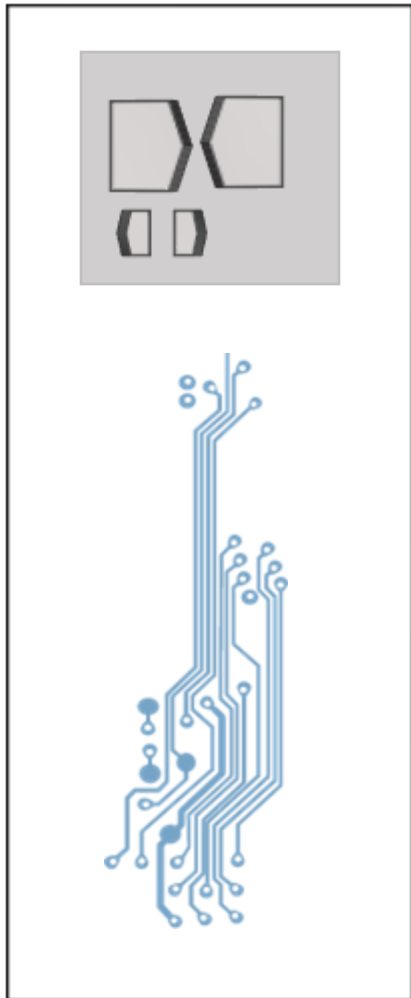
Use default rules for your company.

Setting a package group, enables the Wizard to set the rules regarding it. SOICs, Chips, BGAs and any definition needed.

The Wizard is delivered with predefined settings. To adjust all data preparation to your product you can setup own data preparation Scripts to adjust to your equipment.

# Stencil Generator

## Build in automation support



Set Package Group is only necessary if your data don't contain a proper information. Customers with EPL ("Easylogix Part Library") can resolve trusted data from EPL.

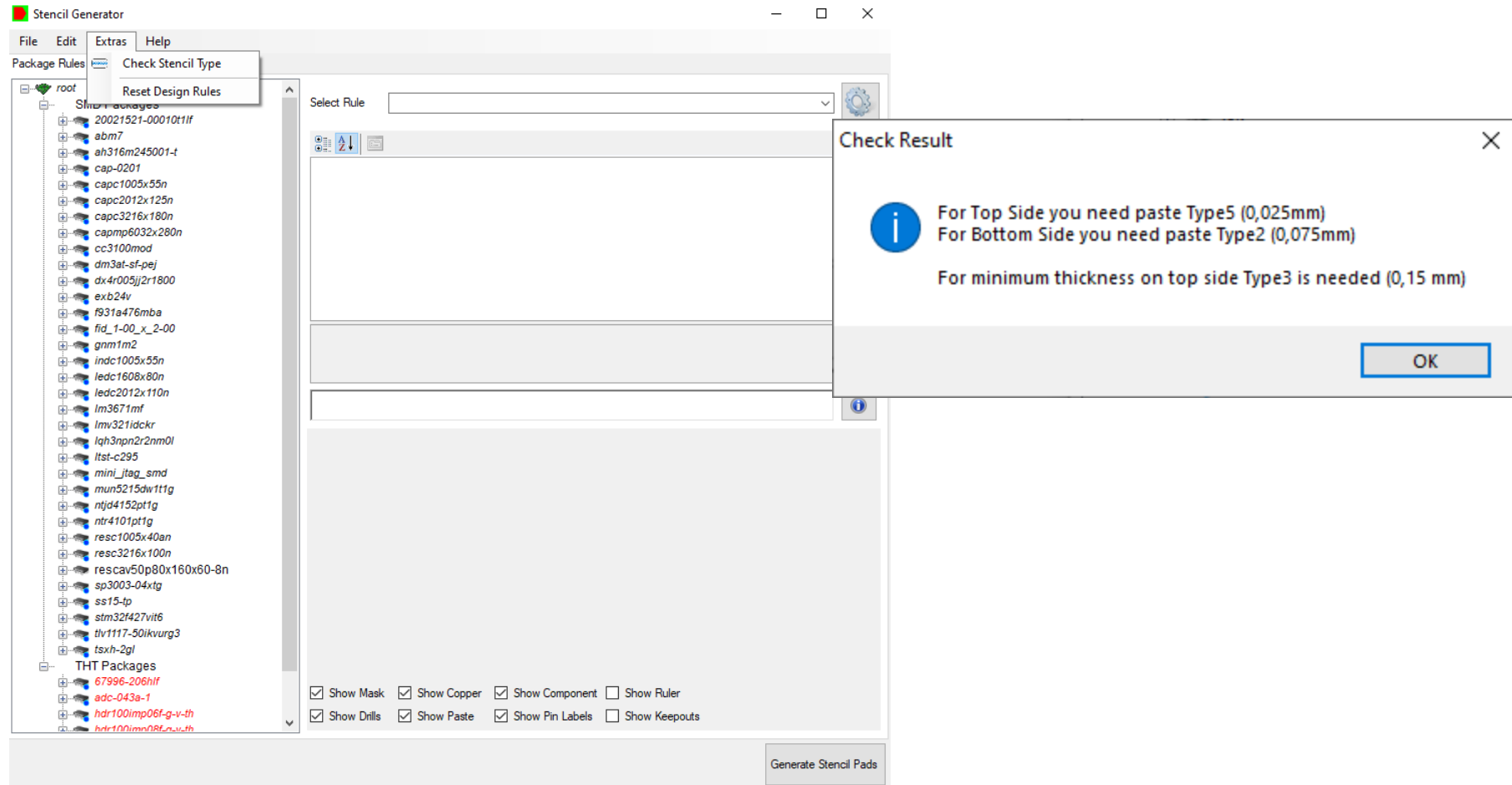
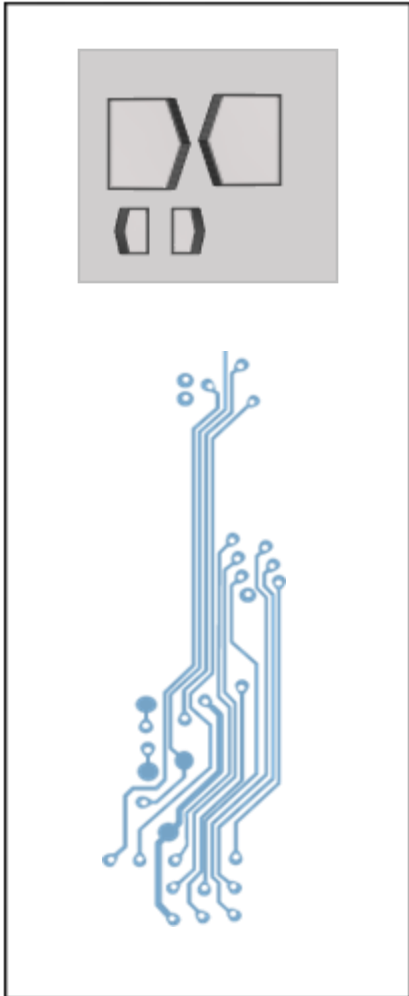
The Wizard also process layouts with multiple mask layers in the stack-up.

Set "Keepouts for Chips" is only available if you have MPN packaged defined. It will handle the usable area for you.

You also can set plugged drills as free usable area.

# Stencil Generator

## Check stencil by using current rules



Stencil Generator

File Edit Extras Help

Package Rules Check Stencil Type

Reset Design Rules

Select Rule

Check Result

For Top Side you need paste Type5 (0,025mm)  
For Bottom Side you need paste Type2 (0,075mm)

For minimum thickness on top side Type3 is needed (0,15 mm)

OK

Generate Stencil Pads

root

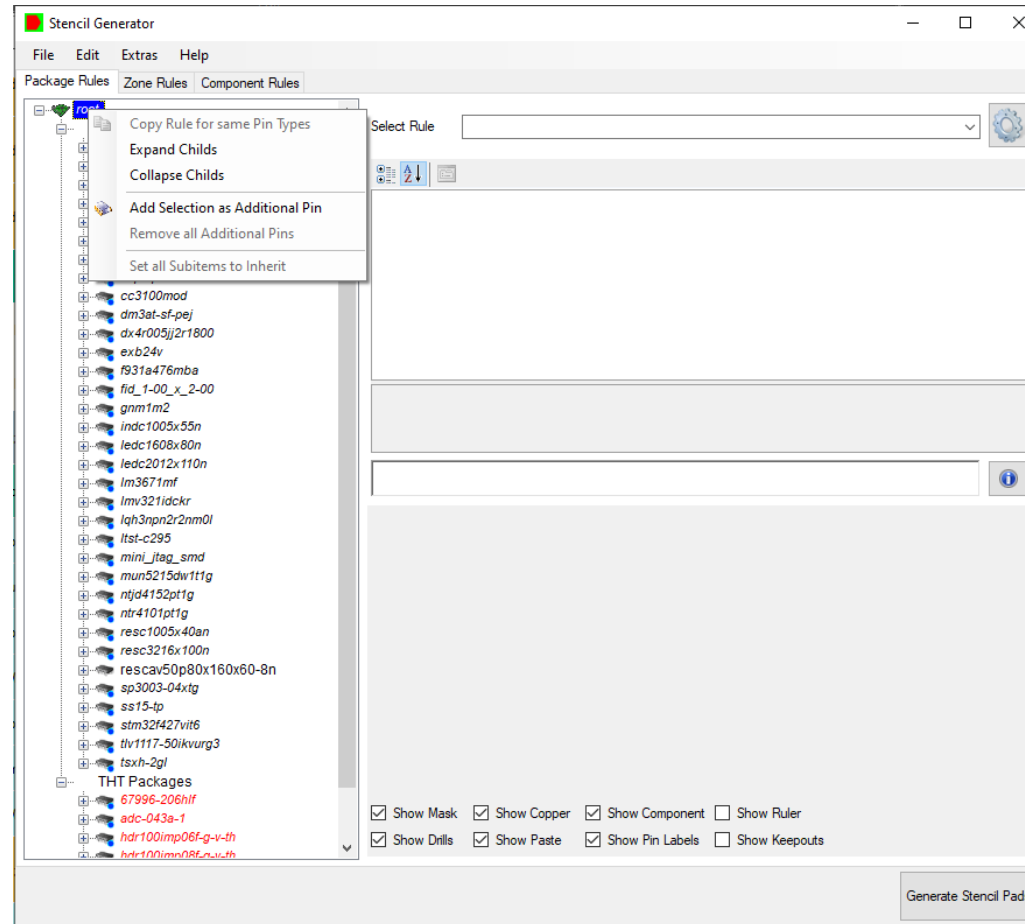
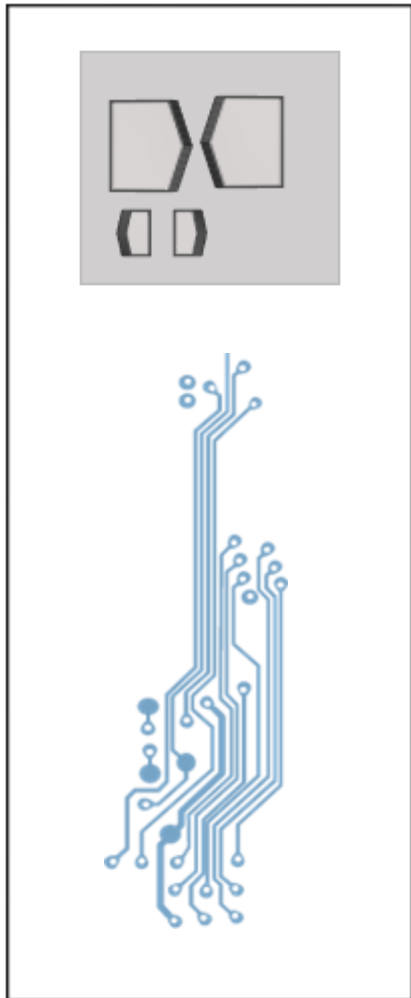
- 20021521-00010t11f
- abm7
- ah316m245001-t
- cap-0201
- capc1005x55n
- capc2012x125n
- capc3216x180n
- capmp6032x280n
- cc3100mod
- dm3at-sf-pej
- dx4r005j2r1800
- exb24v
- f931a476mba
- fid\_1-00\_x\_2-00
- gnm1m2
- indc1005x55n
- ledc1608x80n
- ledc2012x110n
- lm3671mf
- lmv321dckr
- lqh3npn2r2nm0l
- ltst-c295
- mini\_jtag\_smd
- mun5215dw111g
- ntjd4152pt1g
- ntr4101pt1g
- resc1005x40an
- resc3216x100n
- rescav50p80x160x60-8n
- sp3003-04xtg
- ss15-tp
- stm32f427vit6
- tlv1117-50ikvurg3
- tsxh-2gl
- THT Packages
- 67996-206hlf
- adc-043a-1
- hdr100imp06f-g-v-th
- hdr100imp08f-g-v-th

Show Mask Show Copper Show Component Show Ruler

Show Drills Show Paste Show Pin Labels Show Keepouts

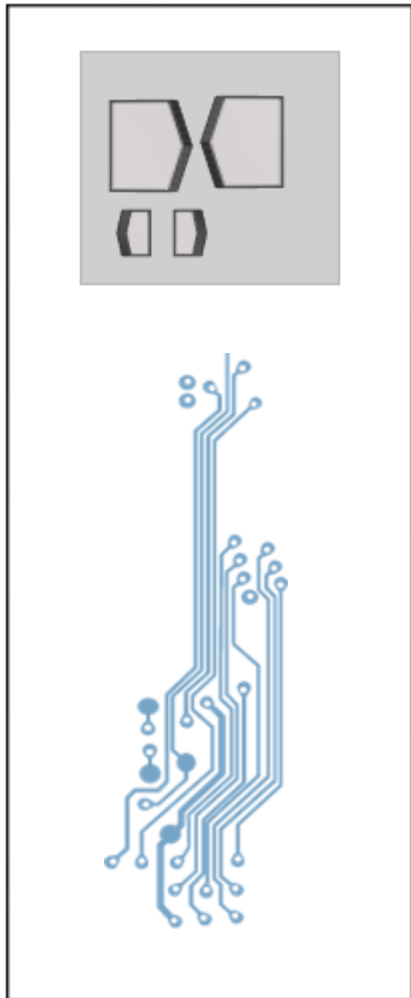
# Stencil Generator

## Crate stencil pin by any drawing



# Stencil Generator

## Rule preview



Stencil Generator

File Edit Extras Help

Package Rules Zone Rules Component Rules

root

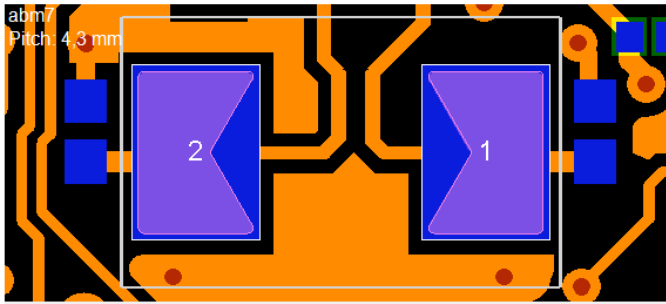
- SMD Packages
  - 20021521-00010t1f
  - abm7**
  - ah316m245001-t
  - cap-0201
  - capc1005x55n
  - capc2012x125n
  - capc3216x180n
  - capmp6032x280n
  - cc3100mod
  - dm3at-sf-pej
  - dx4r005j2r1800
  - exb24v
  - f931a476mba
  - fid\_1-00\_x\_2-00
  - gnm1m2
  - indc1005x55n
  - ledc1608x80n
  - ledc2012x110n
  - lm3671mf
  - lmv321idckr
  - lqh3nqn2r2nm0l
  - ltst-c295
  - mini\_itag\_smd
  - mun5215dw1t1g
  - ntgd4152pt1g
  - ntr4101pt1g
  - resc1005x40an
  - resc3216x100n
  - rescav50p80x160x60-8n
  - sp3003-04xtg
  - ss15-tp
  - stm32f427vit6
  - tlv1117-50kvurg3
  - tsxh-2gl
- THT Packages
  - 67996-206nlf
  - adc-043a-1
  - hdr100imp06f-g-v-th
  - hdr100imp08f-g-v-th

Select Rule: Inherit SMD Packages -> Handle Stencil Creation by Package Group

BGA Threshold Square (MM)	0,4
CHIP Threshold Houses (MM)	2,49
Comer Radius (MM)	0,075
Distance Array Fields (MM)	0,25
House distance cut size in Percent	35
Invert House Pad Direction smaller than (MM)	0,75
Mini Chip Size (MM)	0,075
Minimum Array Field Size (MM)	1,25
Name	Handle Stencil Creation by Package Group
Offset to Center (MM)	0

Name

Handle each stencil generation by package group property, e.g. a CHIP will handled different to SOIC and DPak.



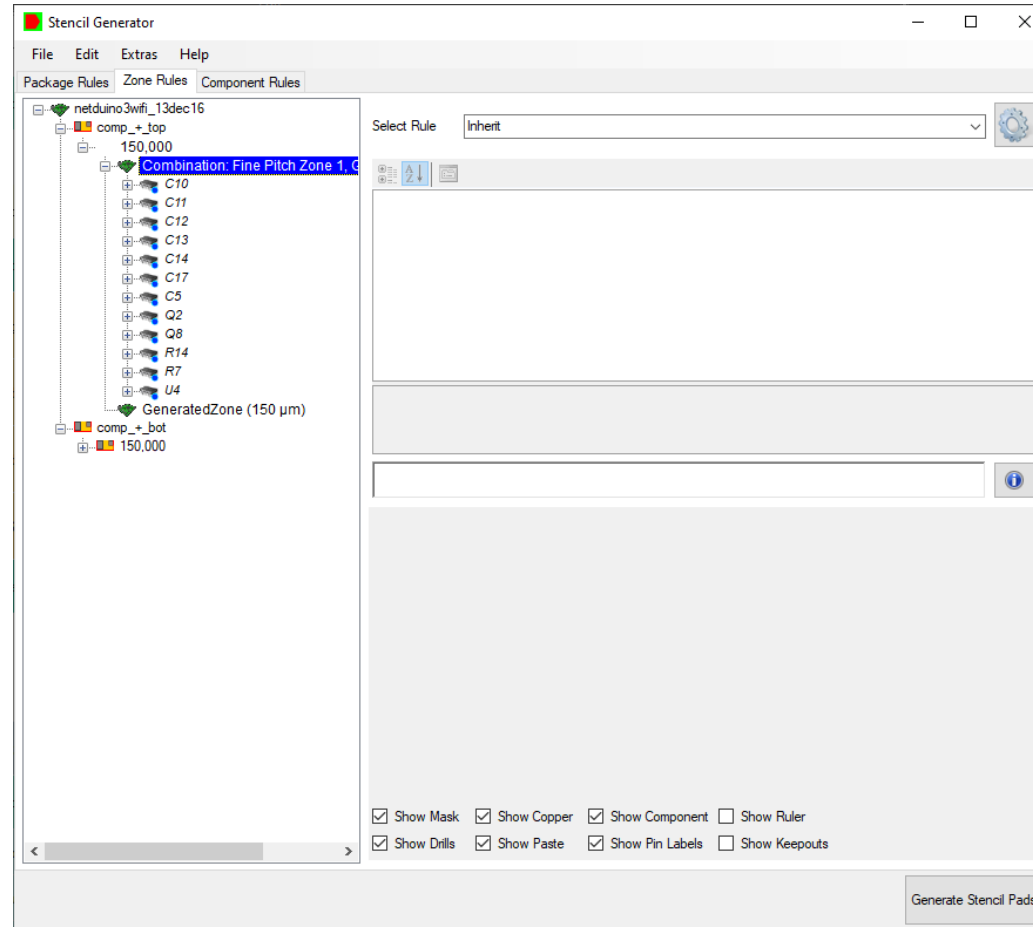
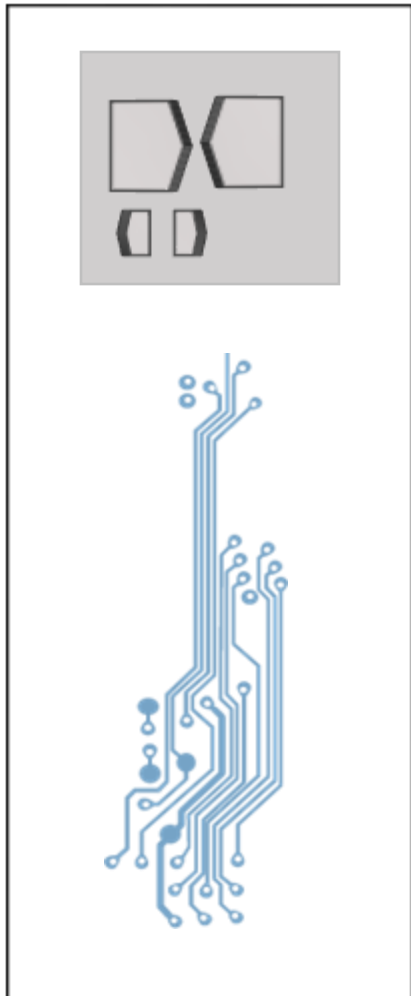
abm7  
Pitch: 4,3 mm

Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

Generate Stencil Pads

# Stencil Generator

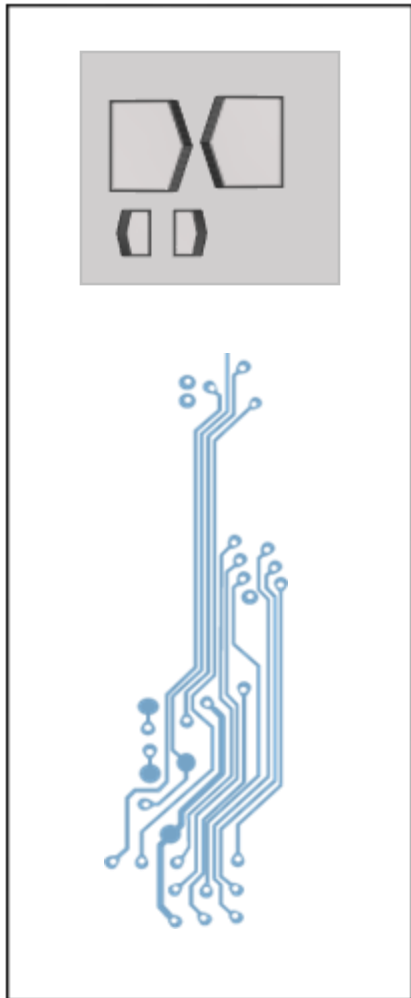
## Set extra rules for components in defined zones





# Stencil Generator

## Set extra rules for components in defined zones



Stencil Generator

File Edit Extras Help

Package Rules Zone Rules Component Rules

netduino3wifi\_13dec16

- comp\_+\_top
  - 150,000
    - Combination: Fine Pitch Zone 1, C
    - C10
    - C11
    - C12
    - C13
    - C14
    - C17
    - C5
    - Q2
    - Q8
    - R14
    - R7
    - U4
  - GeneratedZone (150 µm)
- comp\_+\_bot
  - 150,000

Select Rule

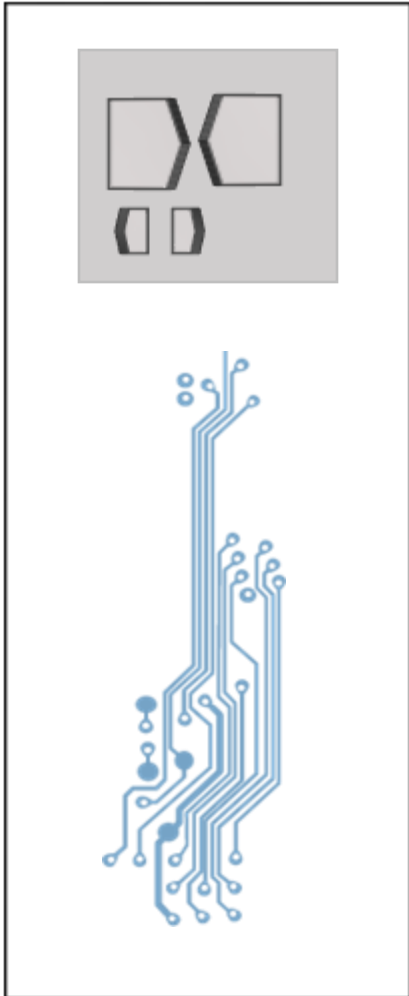
- Inherit
- Ignore
- UndersizeStencilCreationScript
- Donut Creation
- HouseBuilder
- Take Existing Paste Elements
- Handle Stencil Creation by Package Group
- Array Pads
- Array Pads Fix Count
- Use Pin intersecting with Mask
- Free Symbol
- InvertedHouseBuilder

Show Mask
  Show Copper
  Show Component
  Show Ruler  
 Show Drills
  Show Paste
  Show Pin Labels
  Show Keepouts

Generate Stencil Pads

# Stencil Generator

## Set extra rules for components in defined zones



Stencil Generator

File Edit Extras Help

Package Rules Zone Rules Component Rules

netduino3wifi\_13dec16

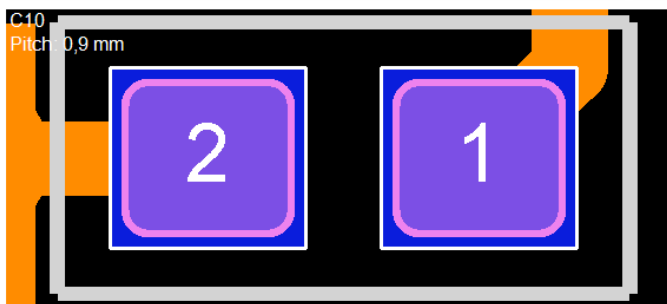
- comp\_+\_top 150,000
  - Combination: Fine Pitch Zone 1, C
  - C10
    - 2(0)
    - 1(1)
  - C11
  - C12
  - C13
  - C14
  - C17
  - C5
  - Q2
  - Q8
  - R14
  - R7
  - U4
- GeneratedZone (150 µm)
- comp\_+\_bot 150,000

Select Rule: Use Pin intersecting with Mask

Corner Radius (MM)	0,075
Name	Use Pin intersecting with Mask
Undersize Value in MM	0,05
Undersize Value in Percent	3,875
Use Fix Undersize Value	True

Name

C10  
Pitch 0,9 mm

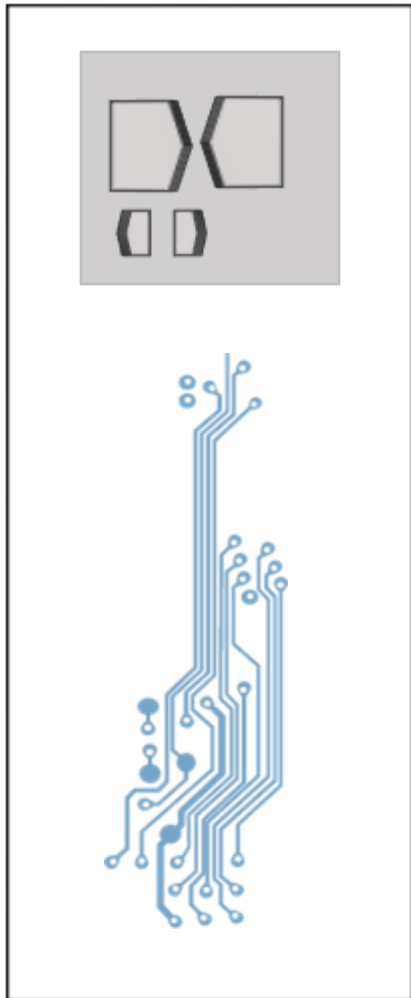


Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

Generate Stencil Pads

# Stencil Generator

## Set extra rules for components in defined zones



Stencil Generator

File Edit Extras Help

Package Rules Zone Rules Component Rules

Filter

comp\_+\_top

- C1
- C10
- C11**
- 2
- 1
- C12
- C13
- C14
- C16
- C17
- C18
- C19
- C2
- C20
- C21
- C22
- C4
- C42
- C43
- C44
- C47
- C48
- C49
- C5
- C50
- C51
- C52
- C53
- C6
- C7
- C9
- D1
- D2
- D3
- D4
- D5
- D6
- D7

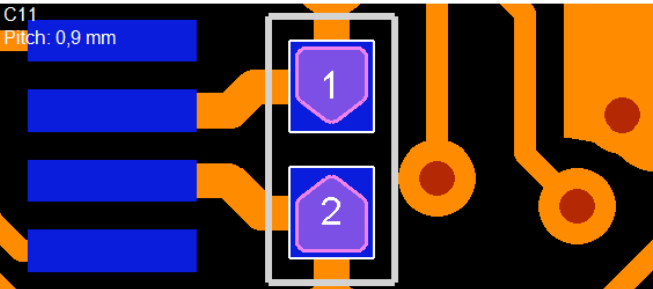
Select Rule: Inherit (Package: capc1005x55n)

BGA Threshold Square (MM)	0.4
CHIP Threshold Houses (MM)	2.49
Corner Radius (MM)	0.075
Distance Array Fields (MM)	0.25
House distance cut size in Percent	35
Invert House Pad Direction smaller than (MM)	0.75
Mini Chip Size (MM)	0.075
Minimum Array Field Size (MM)	1.25
Name	Handle Stencil Creation by Package Group
Offset to Center (MM)	0

Name

Use The component pins and mask to create free areas as stencil pads.

**C11**  
Pitch: 0,9 mm

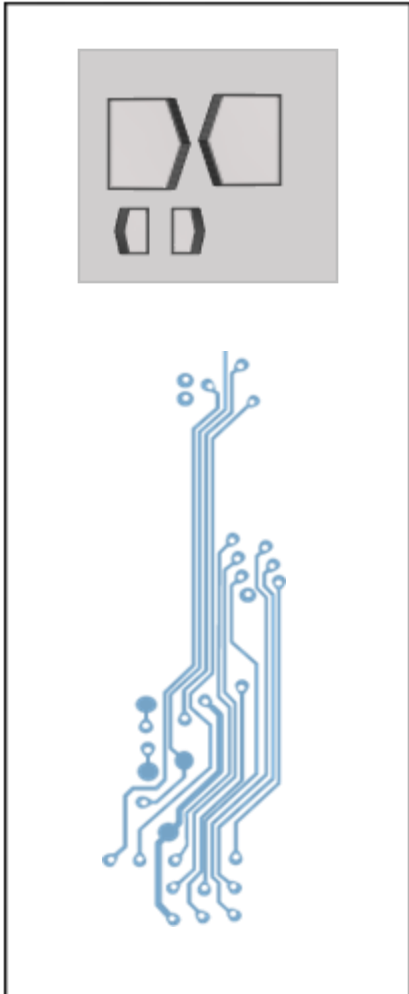


Show Mask  
  Show Copper  
  Show Component  
  Show Ruler  
 Show Drills  
  Show Paste  
  Show Pin Labels  
  Show Keepouts

Generate Stencil Pads

# Stencil Generator

## Integrated measure system in preview



Stencil Generator

File Edit Extras Help

Package Rules Zone Rules Component Rules

Select Rule: Inherit SMD Packages -> Handle Stencil Creation by Package Group

BGA Threshold Square (MM)	0,4
CHIP Threshold Houses (MM)	2,49
Corner Radius (MM)	0,075
Distance Array Fields (MM)	0,25
House distance cut size in Percent	35
Invert House Pad Direction smaller than (MM)	0,75
Mini Chip Size (MM)	0,075
Minimum Array Field Size (MM)	1,25
Name	Handle Stencil Creation by Package Group
Offset to Center (MM)	0

Name

ntr4101pt1g  
Pitch: 1,9 mm

Distance: 1,86 mm

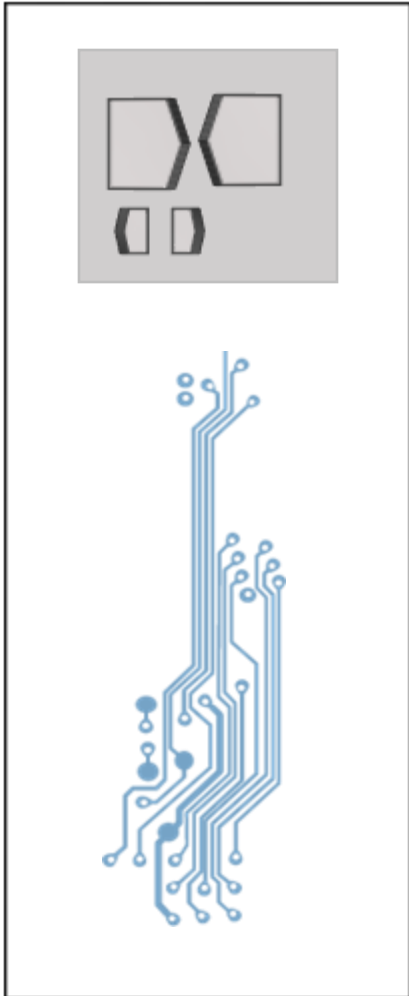
1 2 3

Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

Generate Stencil Pads

- abm7
- ah316m245001-t
- cap-0201
- capc1005x55n
- capc2012x125n
- capc3216x180n
- capmp6032x280n
- cc3100mod
- dm3at-sf-pej
- dx4r005j2r1800
- exb24v
- f931a476mba
- fid\_1-00\_x\_2-00
- gnm1m2
- indc1005x55n
- ledc1608x80n
- ledc2012x110n
- lm3671mf
- lmv321idckr
- lqh3nqn2r2nm0l
- ltst-c295
- mini\_jtag\_smd
- mun5215dw1t1g
- ntjd4152pt1g
- ntr4101pt1g**
- resc1005x40an
- resc3216x100n
- rescav50p80x160x60-8n
- sp3003-04xtg
- ss15-tp
- stm32f427vit6
- tlv1117-50ikvurg3
- tsxh-2gl
- THT Packages
  - 67996-206hlf
  - adc-043a-1
  - hdr100imp06f-g-v-th
  - hdr100imp08f-g-v-th
  - hdr100imp10f-g-v-th
  - mtg320h420np\_720ko

# Stencil Generator



## Take existing paste elements

Select Rule: **Take Existing Paste Elements**

Name: Take Existing Paste Elements

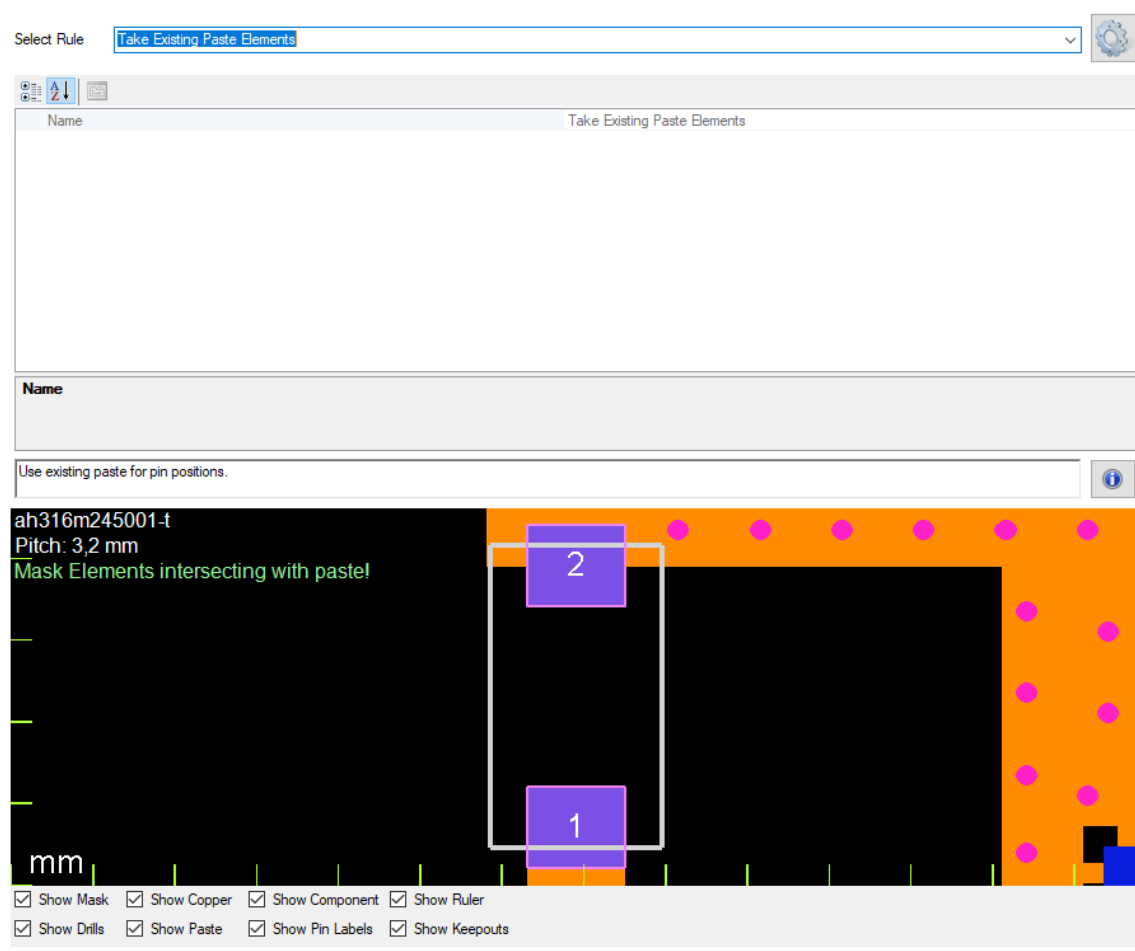
Name:

Use existing paste for pin positions.

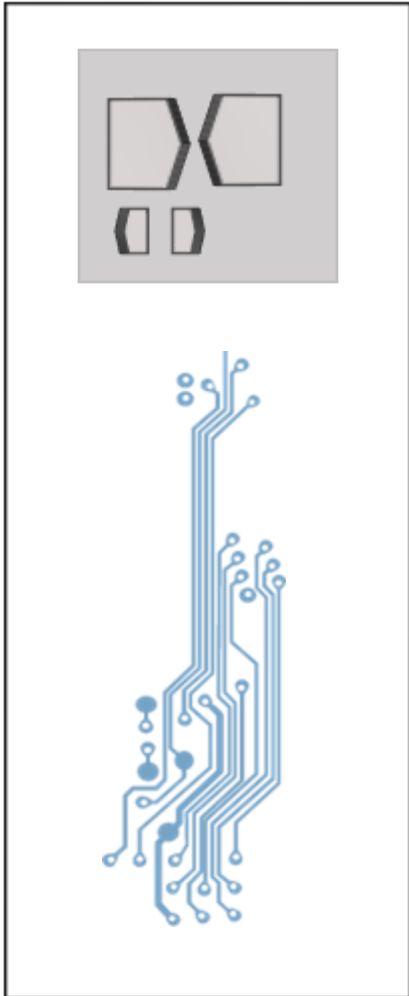
ah316m245001-t  
Pitch: 3,2 mm  
Mask Elements intersecting with paste!

mm

Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts



# Stencil Generator



## Undersize original pads

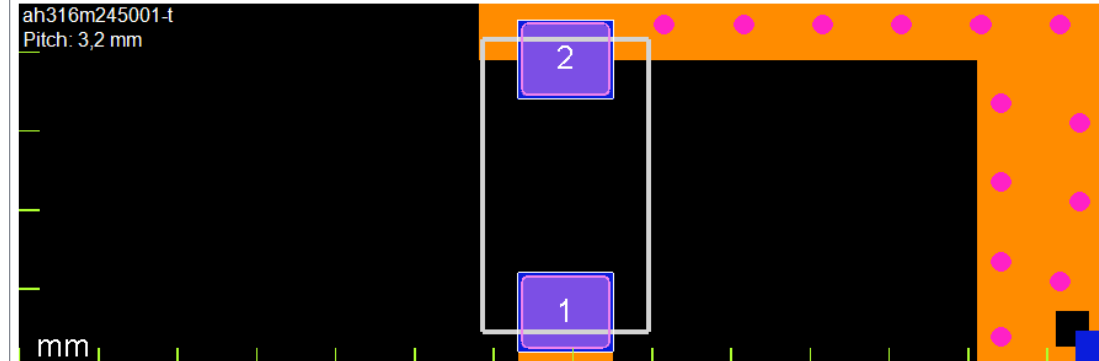
Select Rule: UndersizeStencilCreationScript

Corner Radius (MM)	0.075
Max Size of one Element (MM)	5
Name	UndersizeStencilCreationScript
Steg for Big Elements (MM)	0.75
Undersize Value in MM	0.05
Undersize Value in Percent	1.628

Name

Create undersize for each pin pad with option to switch between fix value in mm and percent value.

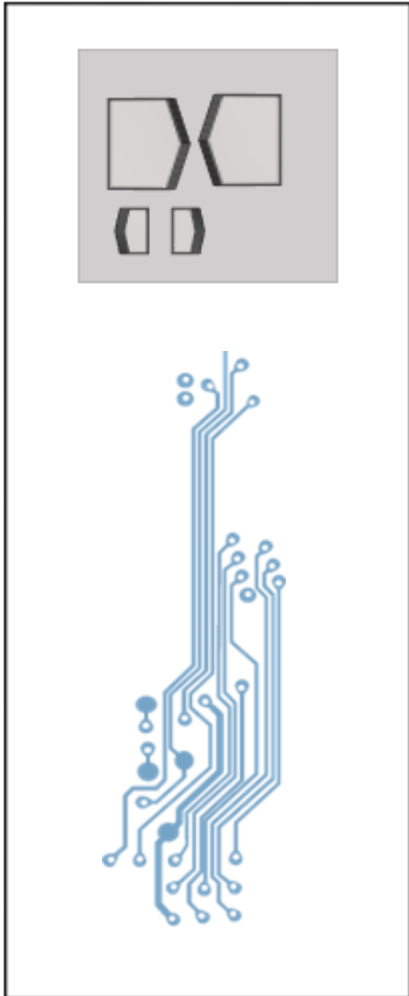
ah316m245001-t  
Pitch: 3,2 mm



Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

Generate Stencil Pads

# Stencil Generator



## Create donat pads

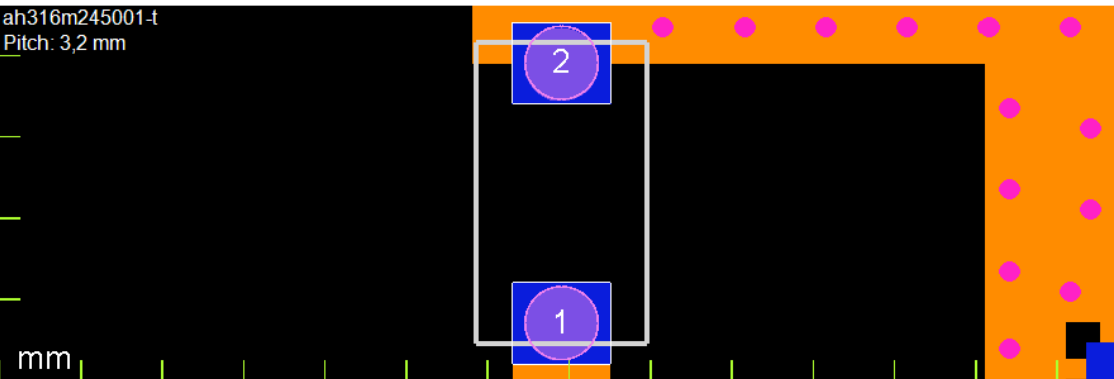
Select Rule: Donut Creation

Corner Radius (MM)	0.075
Count Bridges	4
Name	Donut Creation
Offset to Center X (MM)	0
Offset to Center Y (MM)	0
Size Bridge (MM)	0.5
Undersize Value in MM	0.05
Value for inner donut circle in percent	0.5

Name

Create donut for each pin pad.

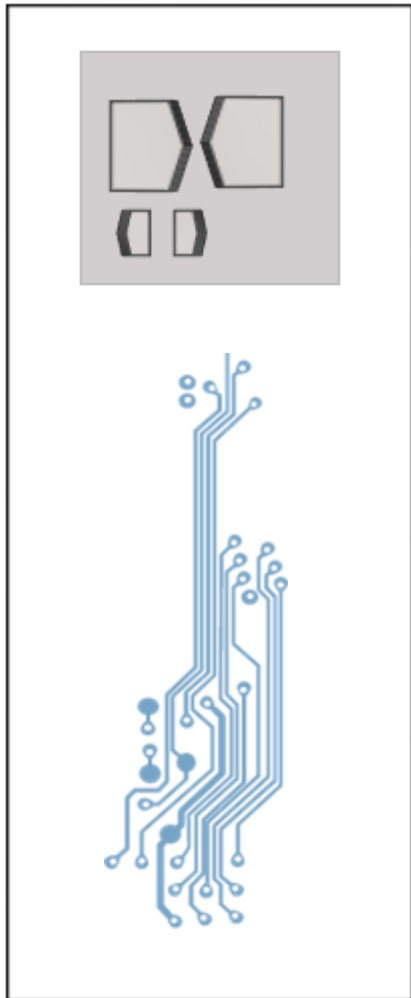
ah316m245001-t  
Pitch: 3,2 mm



mm

Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

# Stencil Generator



## Create house pads

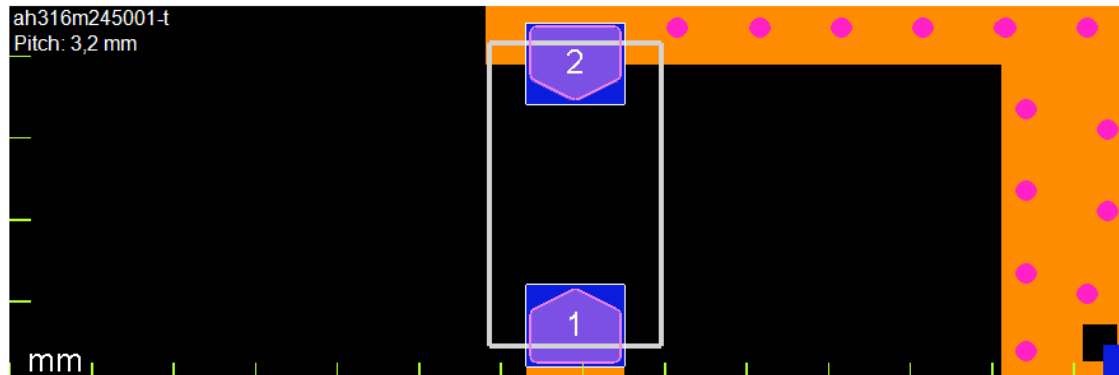
Select Rule:

Corner Radius (MM)	0.075
House distance cut size in Percent	30
Invert Direction	False
Name	HouseBuilder
Offset to Center (MM)	0
Undersize Value (MM)	0.05

**Name**

Create pads in form of small houses.

ah316m245001-t  
Pitch: 3,2 mm

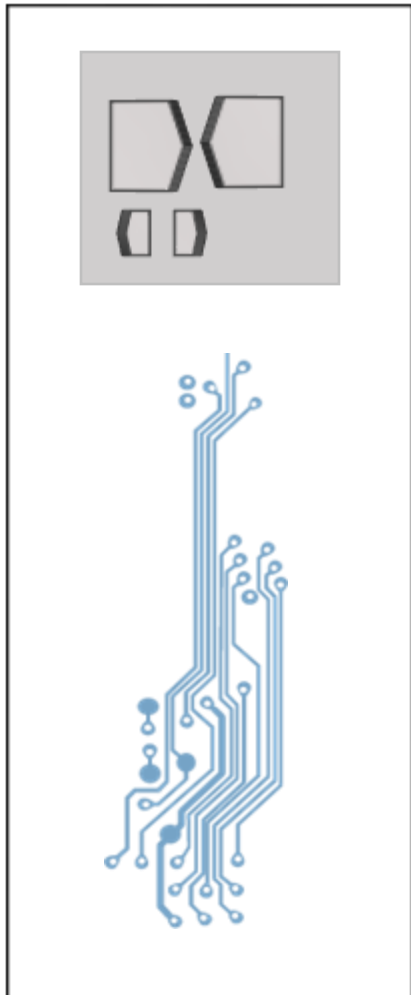


mm

- Show Mask
- Show Copper
- Show Component
- Show Ruler
- Show Drills
- Show Paste
- Show Pin Labels
- Show Keepouts



# Stencil Generator



## Handle pad creation by package group

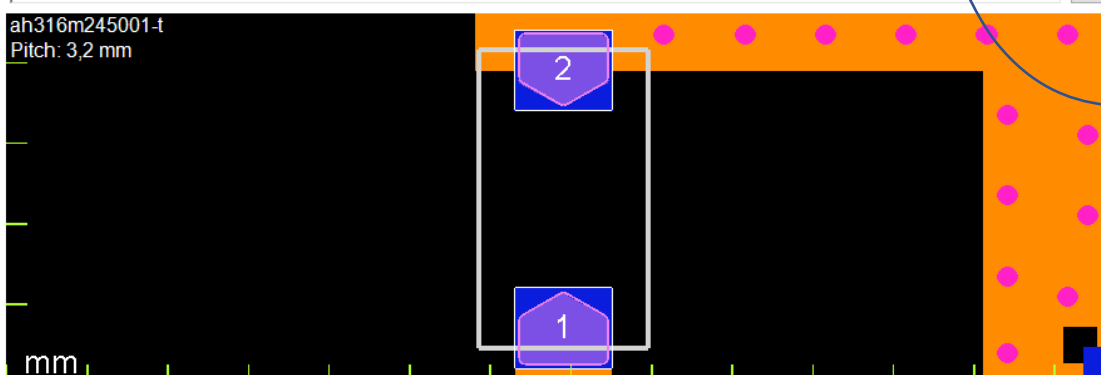
Select Rule: **Handle Stencil Creation by Package Group**

BGA Threshold Square (MM)	0.4
CHIP Threshold Houses (MM)	2.49
Comer Radius (MM)	0.075
Distance Array Fields (MM)	0.25
House distance cut size in Percent	35
Invert House Pad Direction smaller than (MM)	0.75
Mini Chip Size (MM)	0.075
Minimum Array Field Size (MM)	1.25
Name	Handle Stencil Creation by Package Group
Offset to Center (MM)	0
Undersize Value (MM)	0.05
Utilization Array Area (%)	40

Name:

Handle each stencil generation by package group property, e.g. a CHIP will handled different to SOIC and DPak.

ah316m245001-t  
Pitch: 3,2 mm



mm

Show Mask  
  Show Copper  
  Show Component  
  Show Ruler  
 Show Drills  
  Show Paste  
  Show Pin Labels  
  Show Keepouts

Component Properties

Details All Pin Overview

J13

Update with Selection Change

**Component Information**

PartName: HEADER\_2\_0\_AH316M245001-T\_2.45G  
 Reference: J13  
 Variants: (Sammlung)  
 VariantCount: 0  
 Component\_Bounds: [X=-5.800000338, Y=42.099999112, Width=2  
 Component\_CenterPoint: [X=-4.749999898, Y=44.199999992]  
 CompValue: 2.45GHz Antenna  
 IsTop: True  
 Tolerance: -  
 Component\_Height: 0.6  
 Color:   
 PolarityMarker: -1

**Package Information**

UsedPackName: ah316m245001-t

**Transformation**

Position\_X: -4.749999898  
 Position\_Y: 44.199999991999995  
 Rotation: -90  
 MirrorX: False  
 MirrorY: False

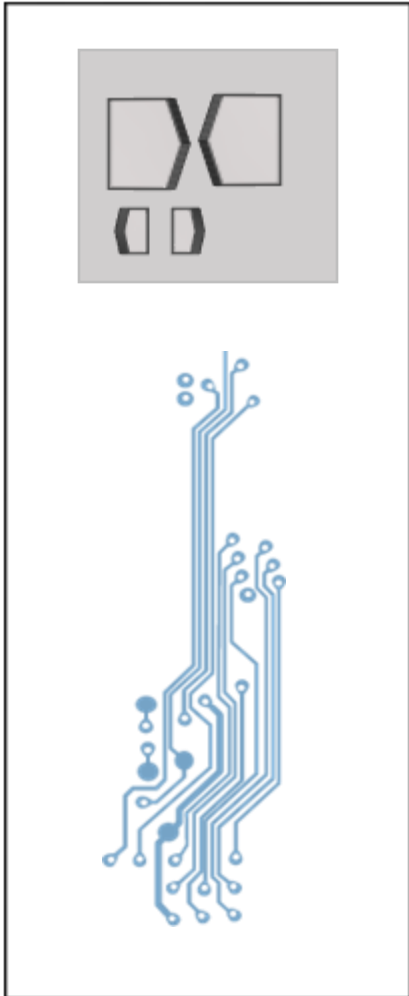
**Position\_X**  
 [read only] Location X of component in selected unit.

Attribute	Value
IPC_Rotation	'90.00'
OemDesignNumberRef	'HEADER_2_0_AH316M245001-T_2.45G'
<b>PACKAGE_GROUP</b>	<b>'CHIP'</b>
Part	'HEADER_2_0_AH316M245001-T_2.45G'
PinCount	'2'
populated	'True'
RefDes	'J13'
VALUE	'2.45GHz Antenna'
Weight	'0'
Height	0.6
Mount Type	SMT

Attribute	Value
Component_Package_Height	0.023620000000000002
InsertCenter_X	0
InsertCenter_Y	0
Package_Bounds	[X=-2.100000088, Y=-1.050000044, Width=4.200
Package_Name	ah316m245001-t
PinCount	2
Pitch	0

Attribute	Value
CadPinType_1	'surface'
CadPinType_2	'surface'
ElectricalType_1	'Electrical'
ElectricalType_2	'Electrical'

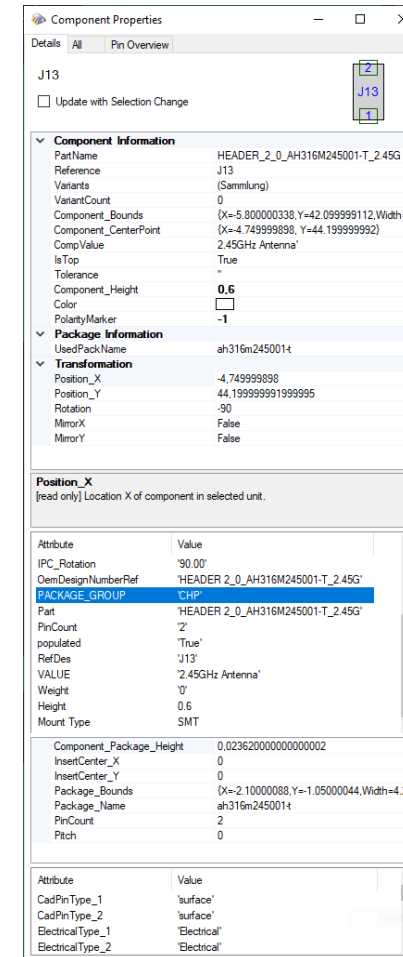
# Stencil Generator



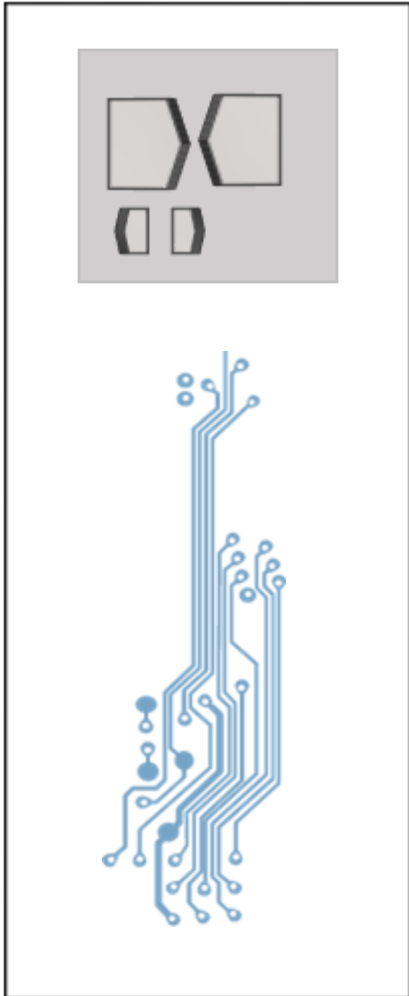
## Handle pad creation by package group

### Predefined package groups

"D_MELF":	"CONNECTOR_SMT":
"R_MELF":	"CONNECTOR_THT":
"SOP":	"FIDUCIAL_CIRCLE":
"QFN":	"FIDUCIAL_RECT":
"QFP":	"FIDUCIAL_CROSS":
"DFN":	"FIDUCIAL":
"SOT":	"LASER":
"SOIC":	"OTHER":
"NETWORK":	"IGNORE":
"SOD":	"DMC":
"C_MOLDED":	"BBS":
"D_MOLDED":	"NOT_PLACED":
"RESISTOR":	"CAE":
"CAPACITOR":	"COIL":
"TANTAL":	"CHP":
"DIODE":	"L_CHP":
"RESONATOR":	"R_CHP":
"INDUCTOR":	"C_CHP":
"DPAK":	"F_CHP":
"LED":	
"C_ARRAY":	
"R_ARRAY":	



# Stencil Generator



## Array pads

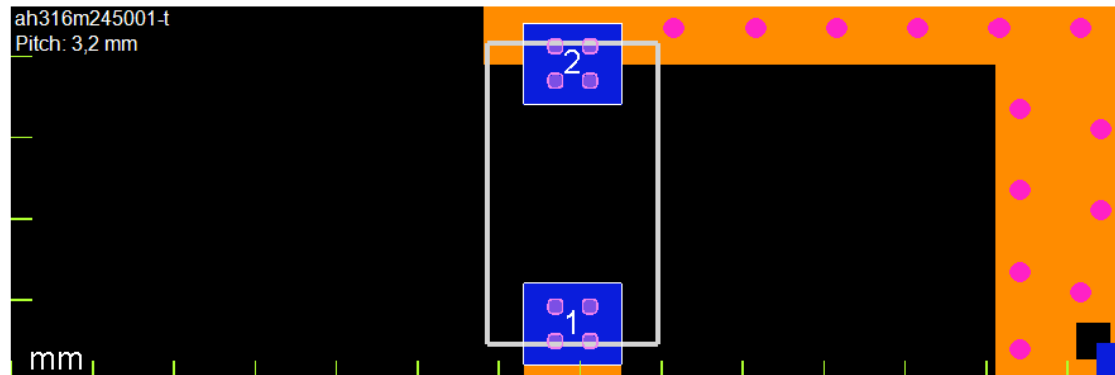
Select Rule: Array Pads

Array Size Height in MM	0,6
Array Size Width in MM	0,6
Corner Radius (MM)	0,05
Distance Array Fields (MM)	0,25
Ignore Mask Intersecting	False
Minimum Array Field Size (MM)	0,1
Name	Array Pads
Offset move away distance (MM)	0
Offset to Center in X direction (MM)	0
Offset to Center in Y direction (MM)	0
Undersize Value in MM	0,05
Utilization Array Area (%)	90

**Utilization Array Area (%)**  
Utilization of available area in percent (only used if no fix size is used and value >0). This option will ignore the undersize value and depending to the settings it is possible the values are not exact.

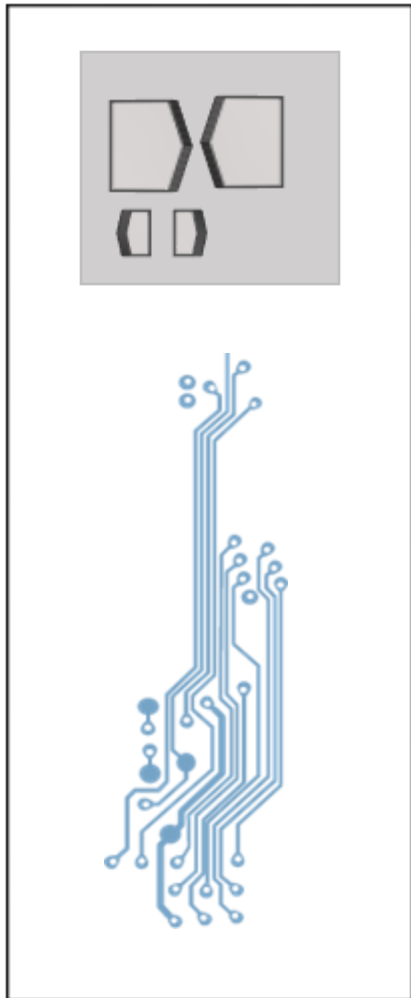
Create array pads, they are cutted by mask opening.

ah316m245001-t  
Pitch: 3,2 mm



Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

# Stencil Generator



## Array pads fixed count

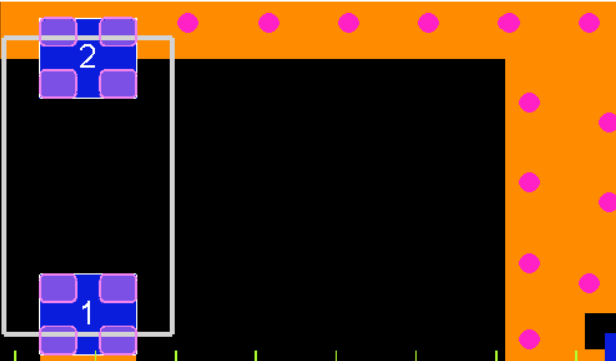
Select Rule: **Array Pads Fix Count**

Array Field Count in X direction	2
Array Field Count in Y direction	2
Array Size Height in MM	2
Array Size Width in MM	2
Corner Radius (MM)	0.075
Distance Array Fields (MM)	0.3
Minimum Array Field Size (MM)	0.5
Name	Array Pads Fix Count
Offset move away distance (MM)	0
Offset to Center in X direction (MM)	0
Offset to Center in Y direction (MM)	0
Undersize Value in MM	0.05

**Name**

Create array pads, with fix count in x and y direction.

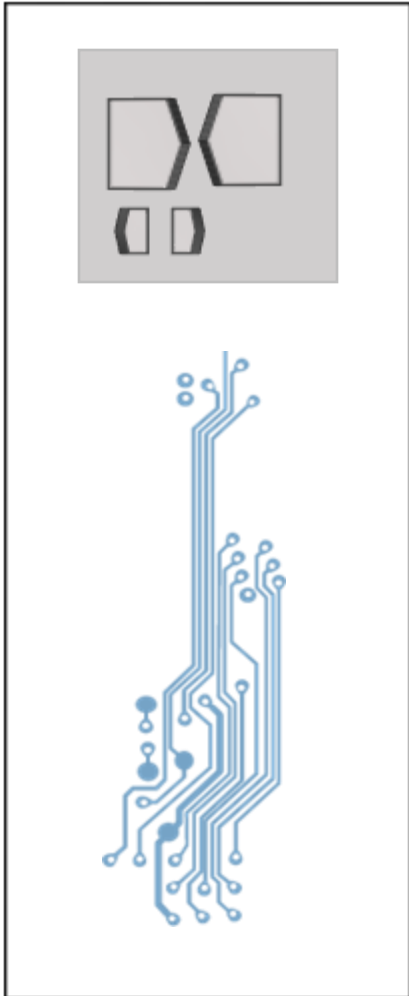
ah316m245001-t  
Pitch: 3,2 mm  
Mask Elements intersecting with paste!



mm

Show Mask  
  Show Copper  
  Show Component  
  Show Ruler  
 Show Drills  
  Show Paste  
  Show Pin Labels  
  Show Keepouts

# Stencil Generator



## Use pin intersecting with solder mask

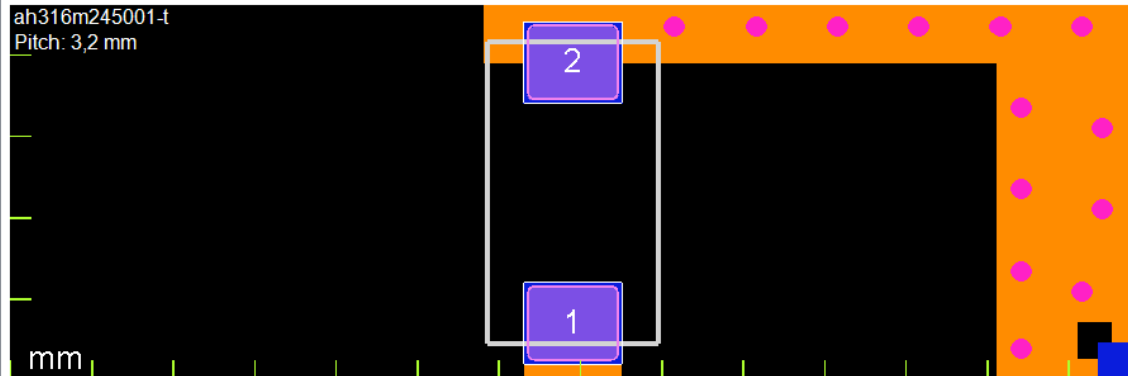
Select Rule: **Use Pin intersecting with Mask**

Corner Radius (MM)	0,075
Name	Use Pin intersecting with Mask
Undersize Value in MM	0,05
Undersize Value in Percent	3,875
Use Fix Undersize Value	True

**Name**

Use The component pins and mask to create free areas as stencil pads.

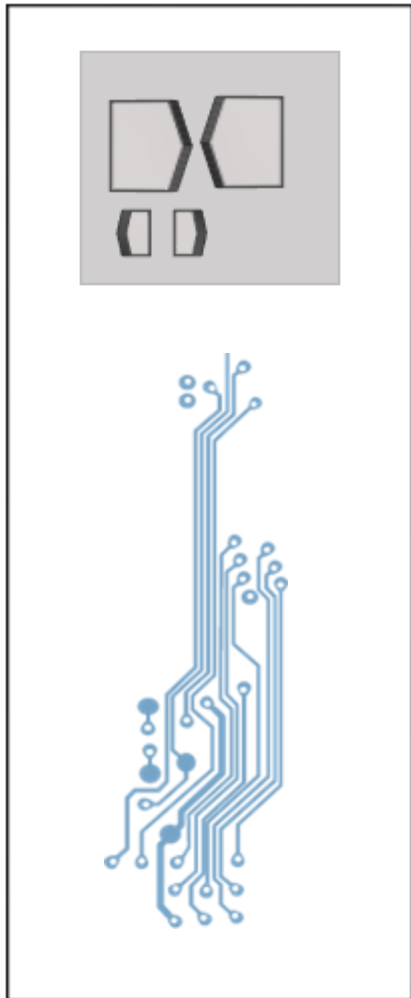
ah316m245001-t  
Pitch: 3,2 mm



mm

Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

# Stencil Generator



## Change symbol

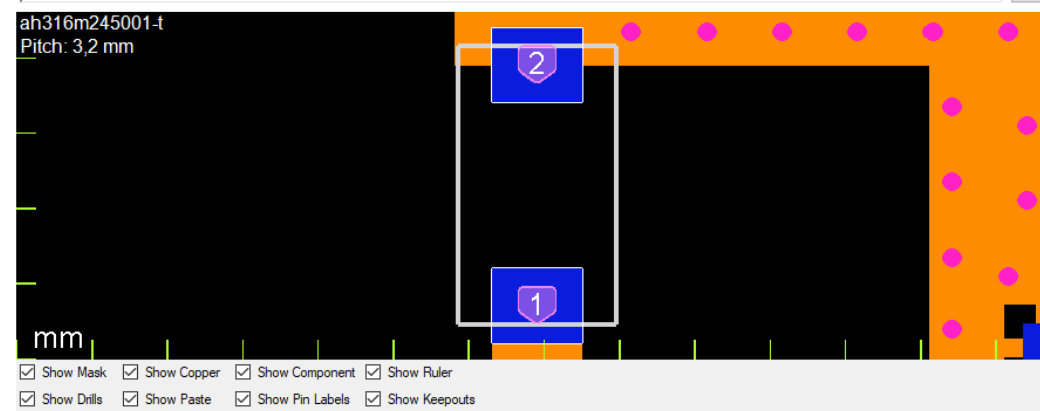
Select Rule: Free Symbol

Name	Free Symbol
Rotation	0
Symbol	<input type="checkbox"/> PCB1_Stencil_Editor.StencilCreationRules.OwnSymbol
HashCode	OwnSymbol
Height	0
Name	
SymbolType	special
Width	0

**Symbol**  
Symbol of the selected object(s)

Select free symbol and place it on the pin location with free rotation.

ah316m245001-t  
Pitch: 3,2 mm




Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

Select a Symbol

Loaded Library: netduino3wfi\_13dec16

ID	Name	Type	Definition
225	r400	r	r15.74803161621...
216	rect450x300	rect	rect17.71654x11.8...
218	rect450x350	rect	rect17.71654x13.7...
115	house_19_685_19_685	special	house_19_685_19_685
32	house_19_685_21_654	special	house_19_685_21_654
45	symbol_305_19_6850421259842x11...	special	symbol_305_19_6850421259842x11...
60	symbol_285_19_6850421259842x11...	special	symbol_285_19_6850421259842x11...
107	symbol_303_19_6850421259842x11...	special	symbol_303_19_6850421259842x11...
171	symbol_306_19_6850421259842x11...	special	symbol_306_19_6850421259842x11...
199	r500	r	r19.68504
226	r500	r	r19.68503952026:
267	rect508x584.2	rect	rect20x23
128	house_21_654_19_685	special	house_21_654_19_685
227	r550	r	r21.65354
1	symbol_213_23_6220521259843x43...	special	symbol_213_23_6220521259843x43...
8	symbol_218_23_6220521259843x43...	special	symbol_218_23_6220521259843x43...
50	symbol_212_23_6220521259843x43...	special	symbol_212_23_6220521259843x43...

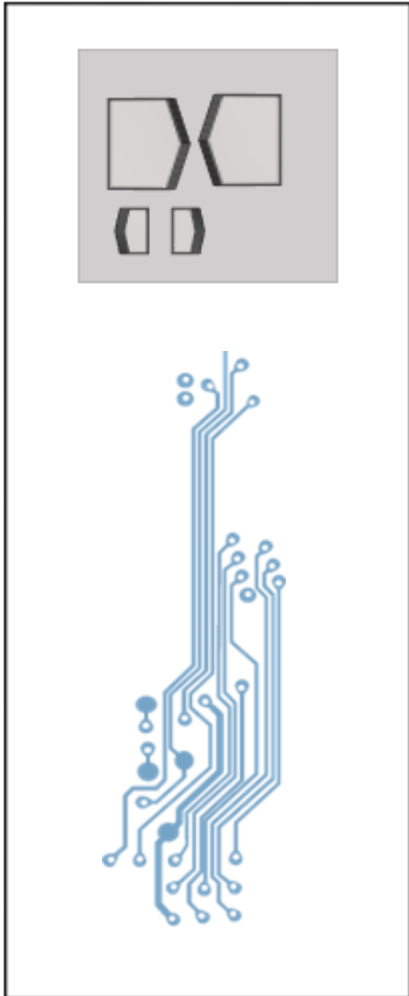
Total: 279 / Filtered: 279 / Selected: 1



Accept

Insert symbols from job or from library

# Stencil Generator



## Inverted house pad

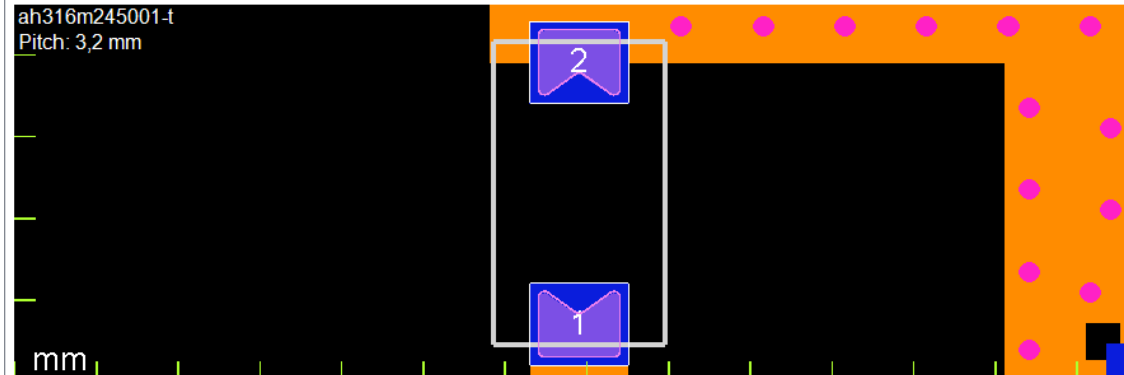
Select Rule:

Corner Radius (MM)	0,075
House distance cut size in Percent	30
Invert Direction	False
Max Size of one Element (MM)	5
Name	InvertedHouseBuilder
Offset to Center (MM)	0
Steg for Big Elements (MM)	0,75
Undersize Value (MM)	0,05

**Name**

Create pads in form of small inverted houses.

ah316m245001-t  
Pitch: 3,2 mm

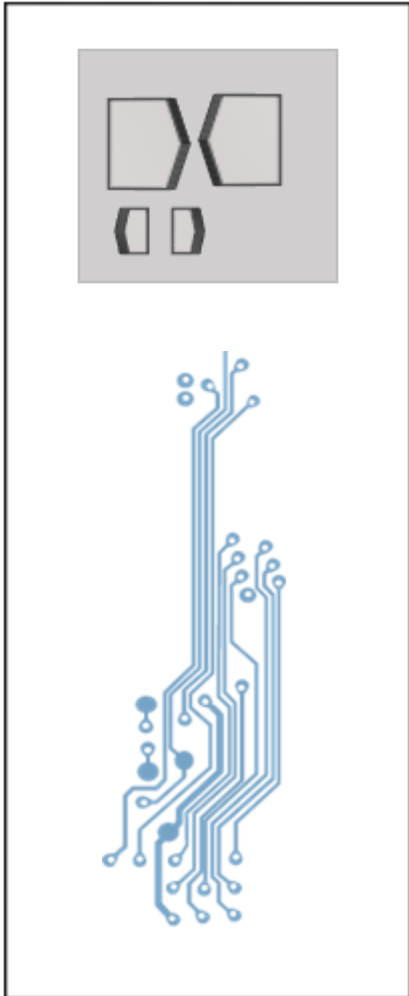
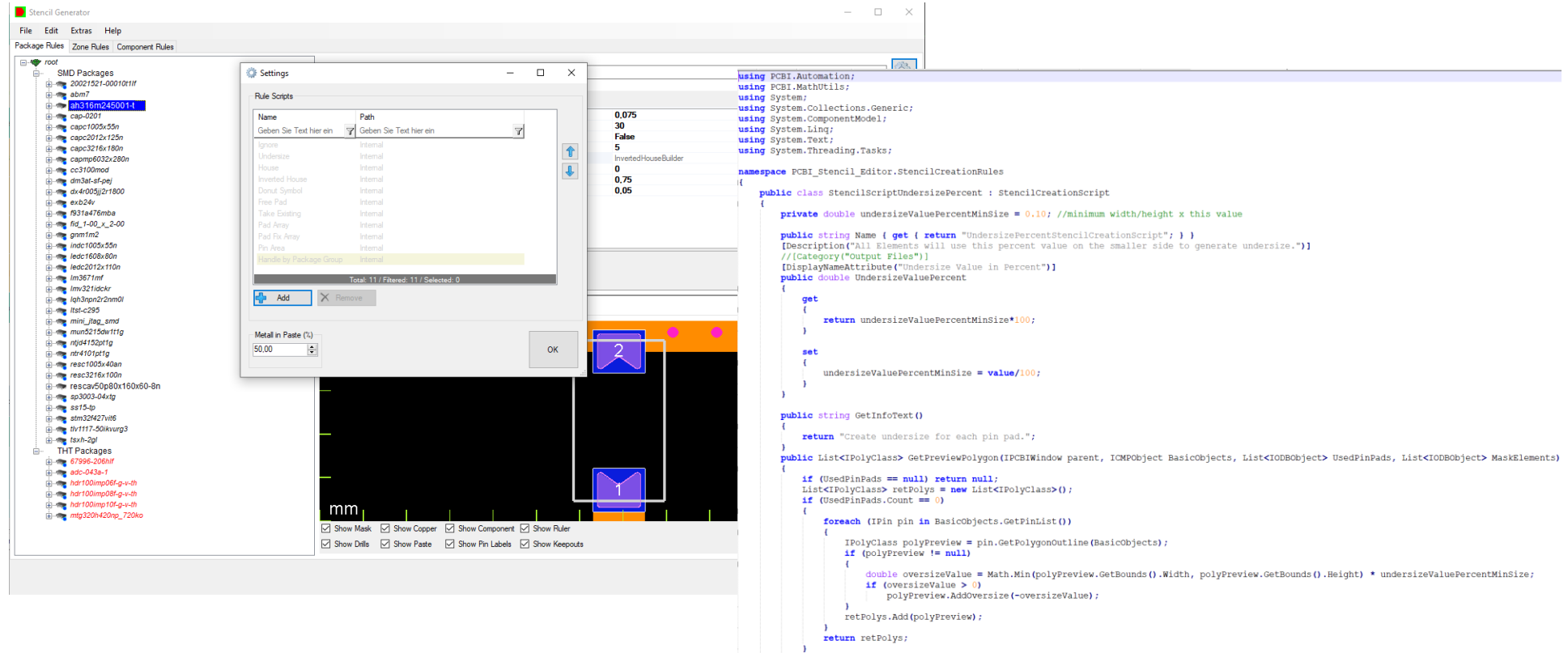


mm

Show Mask  Show Copper  Show Component  Show Ruler  
 Show Drills  Show Paste  Show Pin Labels  Show Keepouts

# Stencil Generator

## Add own rules to your stencil automation

The screenshot shows the Stencil Generator application with the following components:

- File Explorer (Left):** Lists various SMD packages such as 20021521-0001011f, abm7, and 69h315m245001-1.
- Settings Dialog (Center):** A table titled 'Rule Scripts' with columns 'Name' and 'Path'. It lists rules like 'Ignore', 'Undersize', 'House', and 'Inverted House'. A 'Metal in Paste (%)' dropdown is set to 50.00.
- Code Editor (Right):** Shows the C# code for a custom rule script:
 

```
using PCB.Automation;
using PCB.MathUtils;
using System;
using System.Collections.Generic;
using System.ComponentModel;
using System.Linq;
using System.Text;
using System.Threading.Tasks;

namespace PCB_Stencil_Editor.StencilCreationRules
{
    public class StencilScriptUndersizePercent : StencilCreationScript
    {
        private double undersizeValuePercentMinSize = 0.10; //minimum width/height x this value

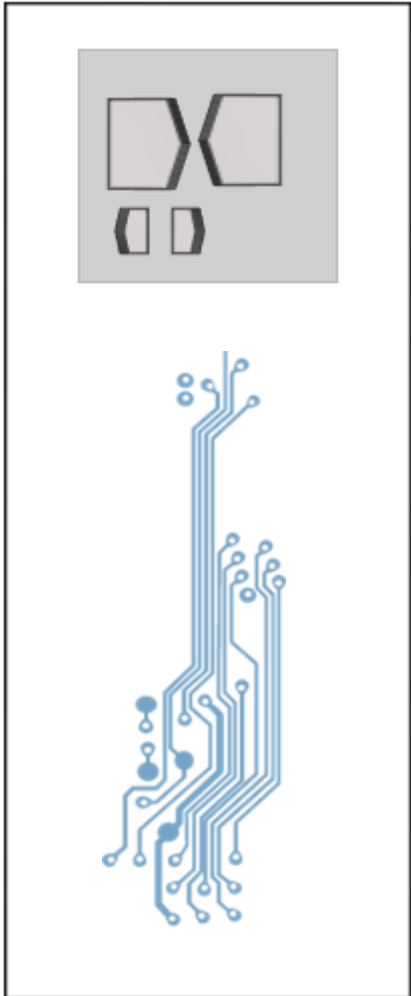
        public string Name { get { return "UndersizePercentStencilCreationScript"; } }
        [Description("All Elements will use this percent value on the smaller side to generate undersize.")]
        //Category("Output Files")
        [DisplayNameAttribute("Undersize Value in Percent")]
        public double UndersizeValuePercent
        {
            get
            {
                return undersizeValuePercentMinSize*100;
            }
            set
            {
                undersizeValuePercentMinSize = value/100;
            }
        }

        public string GetInfoText()
        {
            return "Create undersize for each pin pad.";
        }
        public List<IPolyClass> GetPreviewPolygon(IPCBWindow parent, ICOMObject BasicObjects, List<IODBObject> UsedPinPads, List<IODBObject> MaskElements)
        {
            if (UsedPinPads == null) return null;
            List<IPolyClass> retPolys = new List<IPolyClass>();
            if (UsedPinPads.Count == 0)
            {
                foreach (IPin pin in BasicObjects.GetPinList())
                {
                    IPolyClass polyPreview = pin.GetPolygonOutline(BasicObjects);
                    if (polyPreview != null)
                    {
                        double oversizeValue = Math.Min(polyPreview.GetBounds().Width, polyPreview.GetBounds().Height) * undersizeValuePercentMinSize;
                        if (oversizeValue > 0)
                            polyPreview.AddOversize(-oversizeValue);
                        retPolys.Add(polyPreview);
                    }
                }
            }
            return retPolys;
        }
    }
}
```

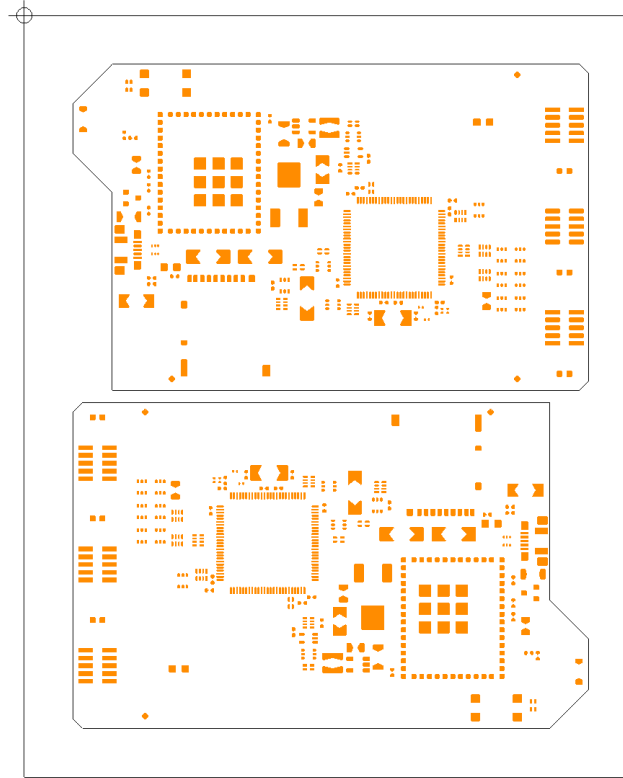
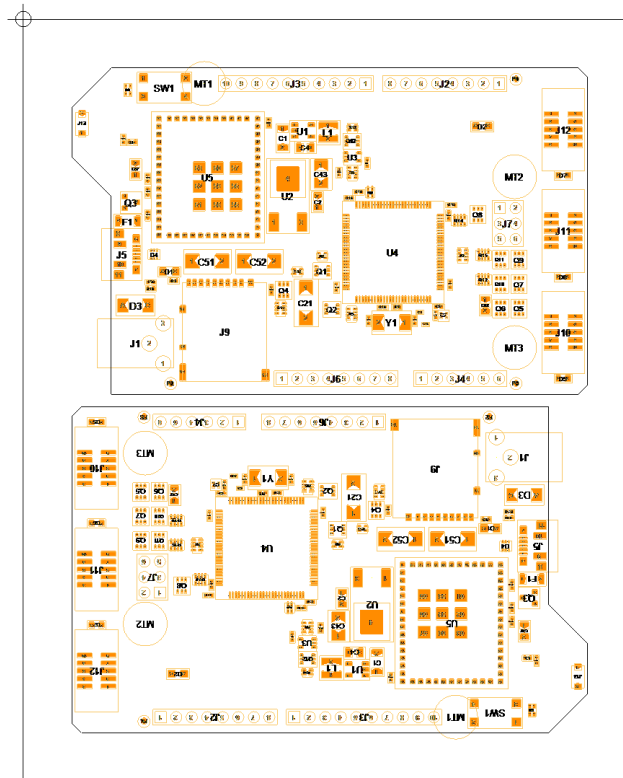
Interface: StencilCreationScript



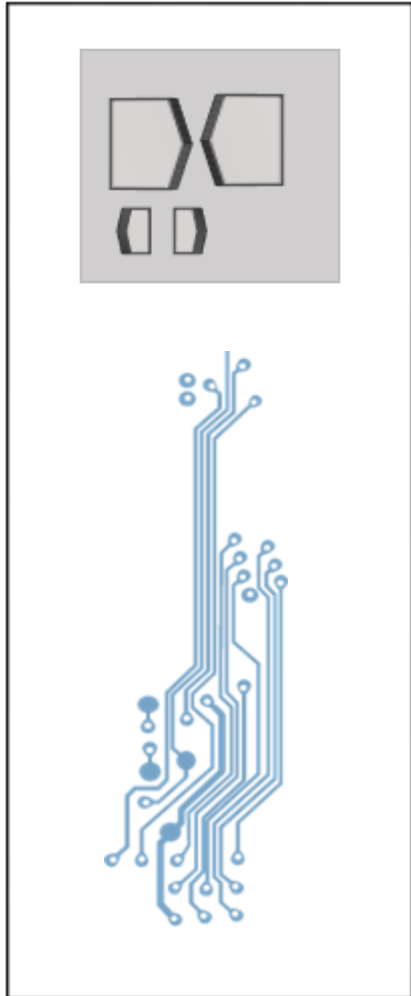
# Panel



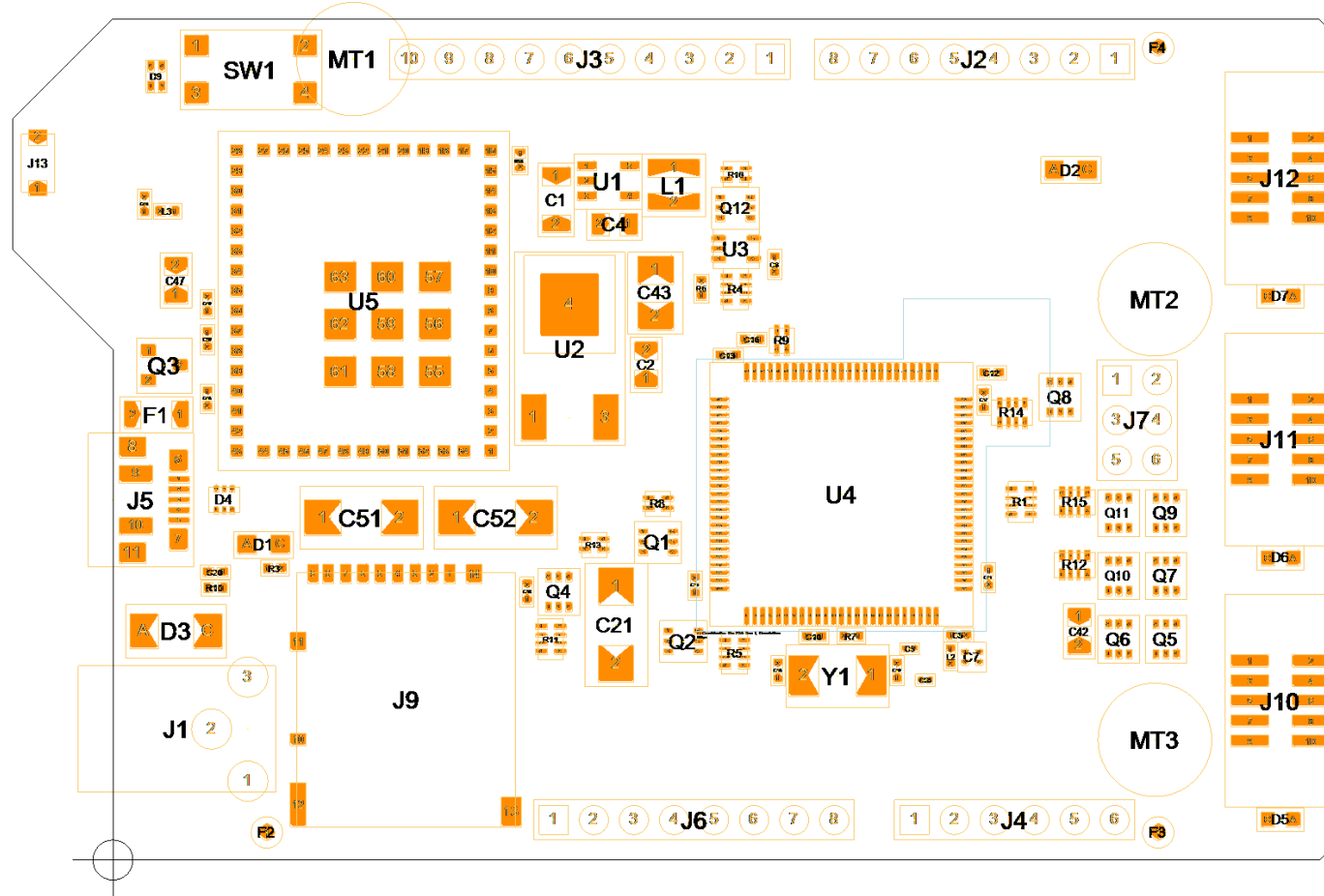
Send the stencil data in your preferred format to your supplier



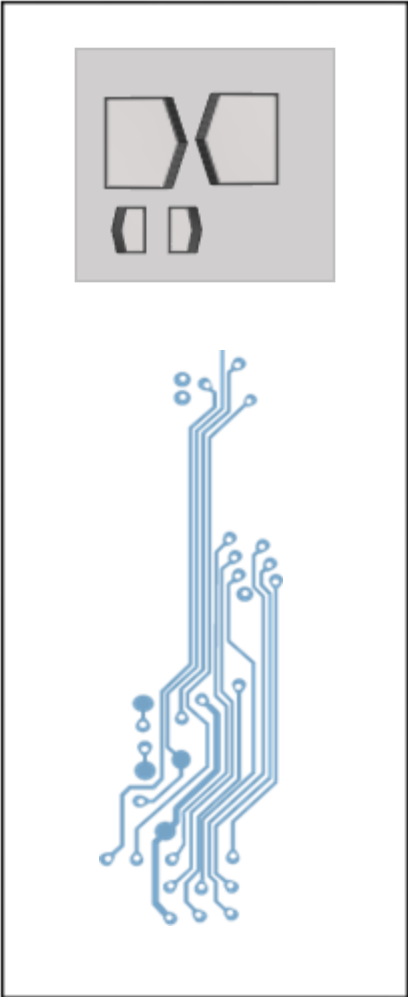
# Stencil Generator



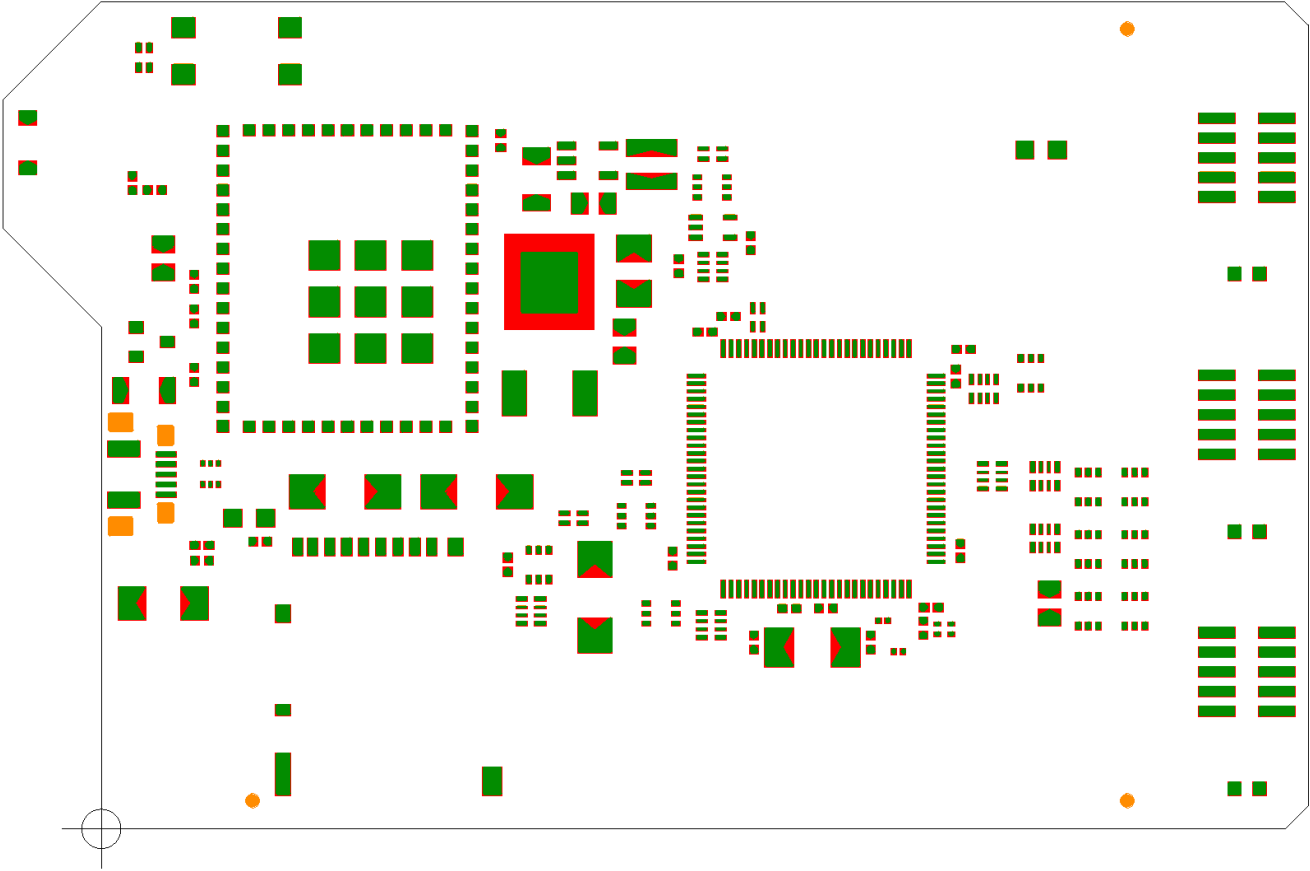
Result of the rule-based stencil wizard



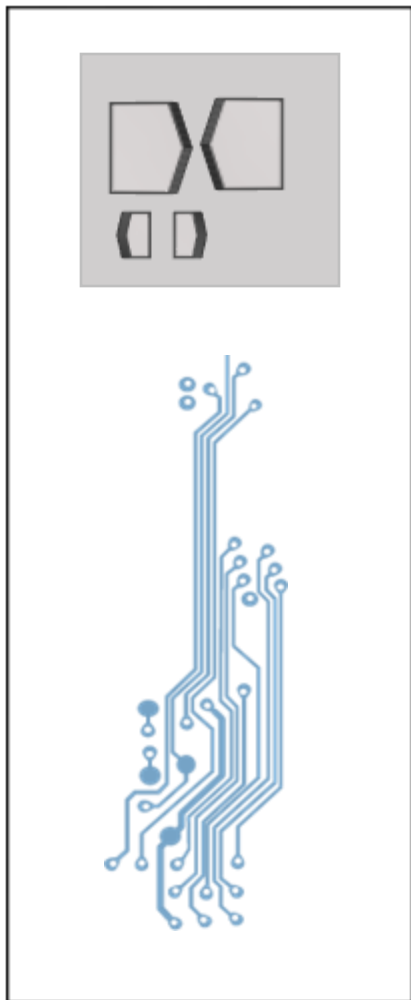
# Stencil Generator



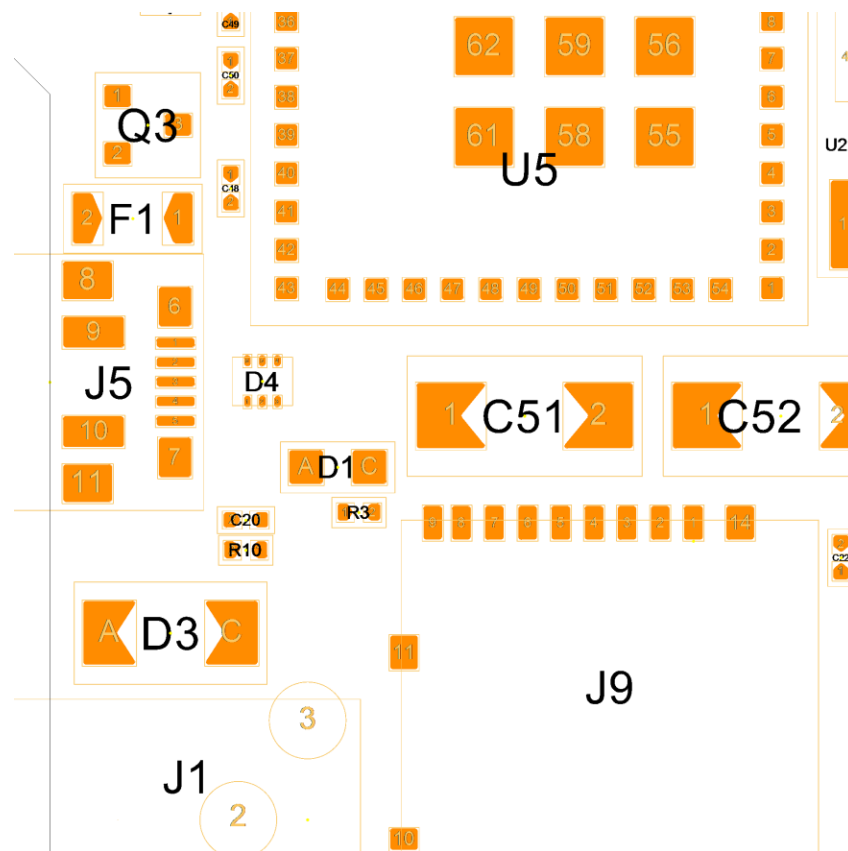
Before and after



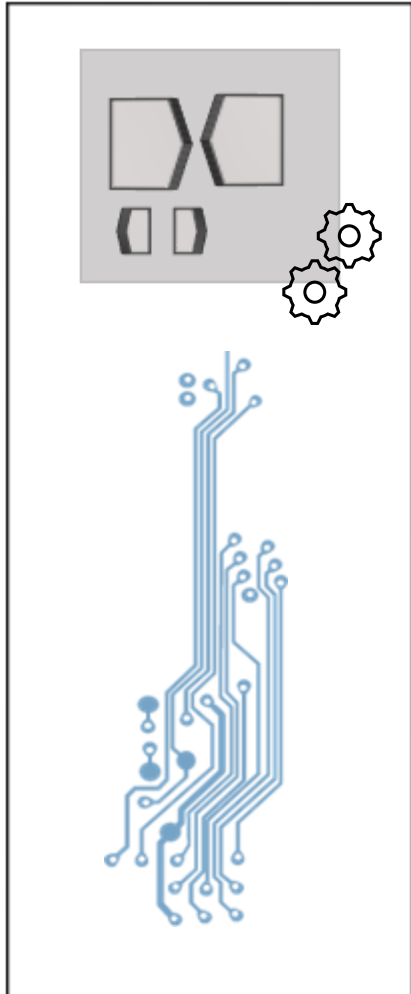
# Stencil Generator



## Stencil pad details



# Stencil Analyzer



Get Paste Size Ratio

File Edit Help

Ratio Help

IPC-7525 May 2000

**Table 1 General Aperture Design Guidelines for Surface-Mount Devices**

Part Type	Pitch	Pad Footprint Width	Pad Footprint Length	Aperture Width	Aperture Length	Stencil Foil Thickness Range	Aspect <sup>2</sup> Ratio Range	Area Ratio Range
PLCC	1.25 mm [49.2 mil]	0.65 mm [25.6 mil]	2.00 mm [78.7 mil]	0.60 mm [23.6 mil]	1.95 mm [76.8 mil]	0.15 - 0.25 mm [5.91 - 9.84 mil]	2.3 - 3.8	0.88 - 1.48
QFP	0.65 mm [25.6 mil]	0.35 mm [13.8 mil]	1.50 mm [59.1 mil]	0.30 mm [11.8 mil]	1.45 mm [57.1 mil]	0.15 - 0.175 mm [5.91 - 6.89 mil]	1.7 - 2.0	0.71 - 0.83
QFP	0.50 mm [19.7 mil]	0.30 mm [11.8 mil]	1.25 mm [49.2 mil]	0.25 mm [9.84 mil]	[1.20 mm] 47.2 mil	0.125 - 0.15 mm [4.92 - 5.91 mil]	1.7 - 2.0	0.69 - 0.83
QFP	0.40 mm	0.25 mm	1.25 mm	0.20 mm	51.20 mm	0.10 - 0.125 mm	1.6 - 2.0	0.68 - 0.86


Stencil thickness: 120  $\mu$ m

Mark lines with ratio <

Use individual Thickness for existing zones

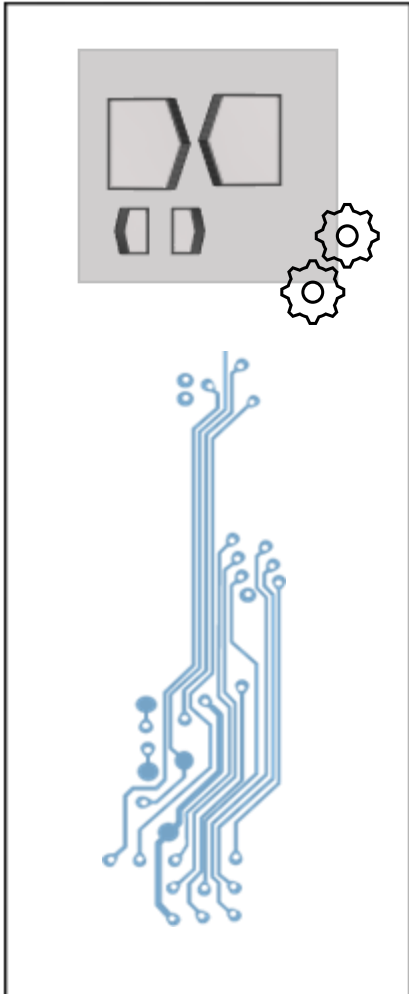
Check only in PCB Profile

Calculate

Export 

Close

# Stencil Ratios



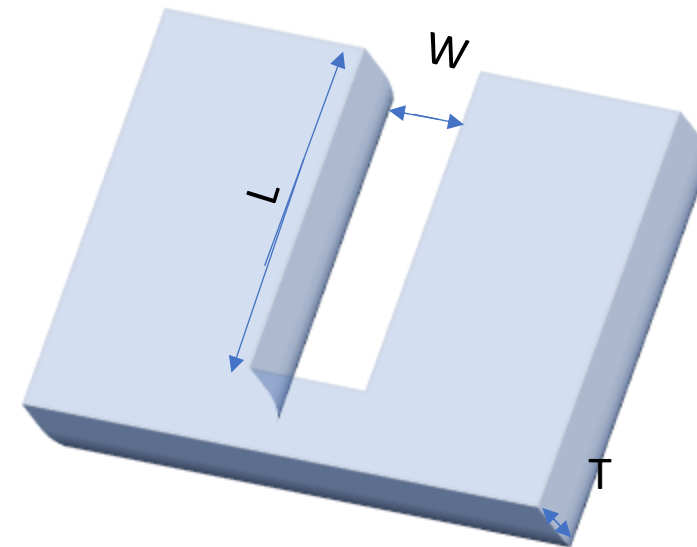
## Solder Paste Stencil Ratios

In order to ensure efficient transfer of solder paste from a stencil aperture to a pad during the soldering process, there are two main ratios to consider:

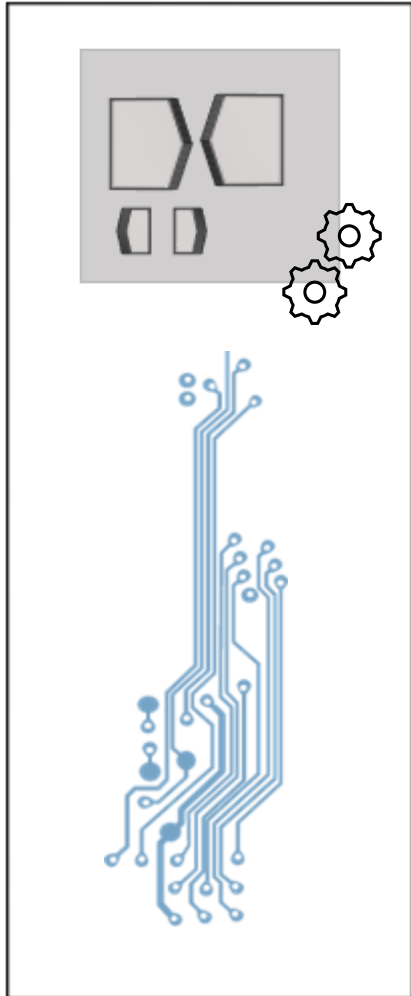
- **Aspect ratio:** the relation between the width of narrowest aperture and the thickness of the stencil. This ratio should be at least 1.5.
- **Area ratio:** gives a more accurate and detailed indication of a stencil's paste release performance. This is the ratio between the area of the aperture and the area of the hole walls. This ratio should be at least 0.66.

$$\text{Aspect Ratio} = W / T$$

$$\text{Area Ratio} = A (\text{Pad}) / A (\text{Wall})$$



# Stencil analyzer



Stencil Analysis

File Edit Help

Check Ratio Rules

Aspect Ratio (Area/Thickness) > 1.50

Area Ratio (Area/Wall) > 0.66

Check Solder Paste Type Rules

Default Ball Rule >= 5

Round Ball Rule (Symbol r) >= 7

Prefered Solder Paste Type: Type4 (38,000 micron)

Check Pin Gap Rules

Size of gaps between pins >= pitch 50.00 %

Maximum Pad Size (smallest side) 0.750 mm

Check Metal in Paste Volumen Rules

Material Volume < 6.50

Material Volume > 3.50

Metal in Solder Paste 50.00 %

Check Squeegee Direction Rules

Squeegee Direction  Bottom Top  Left Right

Zone Distance Definitions

Stencil Thickness

Default thickness 195 µm

Use individual Thickness for existing zones

Component	Pin	Status	Area Ratio	Aspect Ratio	Area	Area Walls	Paste Type	Metal in Solder	Squeegee Rule	Pitch Rule	X	Y	Width	Height	Stencil Thickness	Paste Volume	Symbol	Geometry
T8206_LU	1	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	161.309	43.274	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T8205_LU	3	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	155.621	43.989	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T8205_LU	2	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	153.421	43.039	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T8205_LU	1	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	153.421	44.939	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T8001_LU	3	Not OK	1.496	5.128	1.400	0.936	OK	OK	OK	OK	165.805	11.482	1000.0 µm	1400.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T8001_LU	2	Not OK	1.496	5.128	1.400	0.936	OK	OK	OK	OK	164.855	13.682	1000.0 µm	1400.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T8001_LU	1	Not OK	1.496	5.128	1.400	0.936	OK	OK	OK	OK	166.755	13.682	1000.0 µm	1400.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
D5314	3	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	249.181	34.212	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
D5314	2	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	251.381	35.162	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
D5314	1	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	251.381	33.262	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T5235	3	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	206.103	-11.403	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T5235	2	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	203.903	-12.353	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
T5235	1	Not OK	1.496	7.179	1.400	0.936	OK	OK	OK	OK	203.903	-10.453	1400.0 µm	1000.0 µm	195.0 µm	0.273 mm³	rect55.118110...	
J1305	10	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	193.247	-63.410	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	9	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	189.817	-63.410	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	8	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	193.247	-62.140	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	7	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	189.817	-62.140	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	6	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	193.247	-60.870	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	5	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	189.817	-60.870	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	4	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	193.247	-59.600	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	3	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.530 mm(<0.635)	189.817	-59.600	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	2	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.510 mm(<0.635)	193.247	-58.330	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
J1305	1	OK	1.514	14.974	2.161	1.427	OK	OK	OK	0.510 mm(<0.635)	189.817	-58.330	2920.0 µm	740.0 µm	195.0 µm	0.421 mm³	rect114.96059...	
T1205	3	OK	1.518	5.128	1.450	0.956	OK	OK	OK	OK	265.579	-83.768	1000.0 µm	1450.0 µm	195.0 µm	0.283 mm³	rect57.086612...	
T1205	2	OK	1.518	5.128	1.450	0.956	OK	OK	OK	OK	263.289	-83.768	1000.0 µm	1450.0 µm	195.0 µm	0.283 mm³	rect57.086612...	
T1205	1	OK	1.518	5.128	1.450	0.956	OK	OK	OK	OK	260.999	-83.768	1000.0 µm	1450.0 µm	195.0 µm	0.283 mm³	rect57.086612...	
U5106	3	OK	1.518	7.436	1.450	0.956	OK	OK	OK	OK	216.315	31.393	1450.0 µm	1000.0 µm	195.0 µm	0.283 mm³	rect57.086612...	
U5106	2	OK	1.518	7.436	1.450	0.956	OK	OK	OK	OK	216.315	33.683	1450.0 µm	1000.0 µm	195.0 µm	0.283 mm³	rect57.086612...	
U5106	1	OK	1.518	7.436	1.450	0.956	OK	OK	OK	OK	216.315	35.973	1450.0 µm	1000.0 µm	195.0 µm	0.283 mm³	rect57.086612...	
L1701	2	OK	1.524	4.615	1.575	1.033	OK	OK	OK	OK	267.444	-73.607	900.0 µm	1750.0 µm	195.0 µm	0.307 mm³	rect68.897598...	
L1701	1	OK	1.524	4.615	1.575	1.033	OK	OK	OK	OK	264.244	-73.607	900.0 µm	1750.0 µm	195.0 µm	0.307 mm³	rect68.897598...	

Total: 5688 / Filtered: 5688 / Selected: 0

Zone Issue Distance Check Value Step

Gegeben Sie Text hier ein Gegeben Sie Text Gegeben Sie Text Gegeben Sie Text

No Zone Step issue found

Total: 0 / Filtered: 0 / Selected: 0

Options

Filter Layers

TOP 377669-1.GBX

Check only in PCB Profile

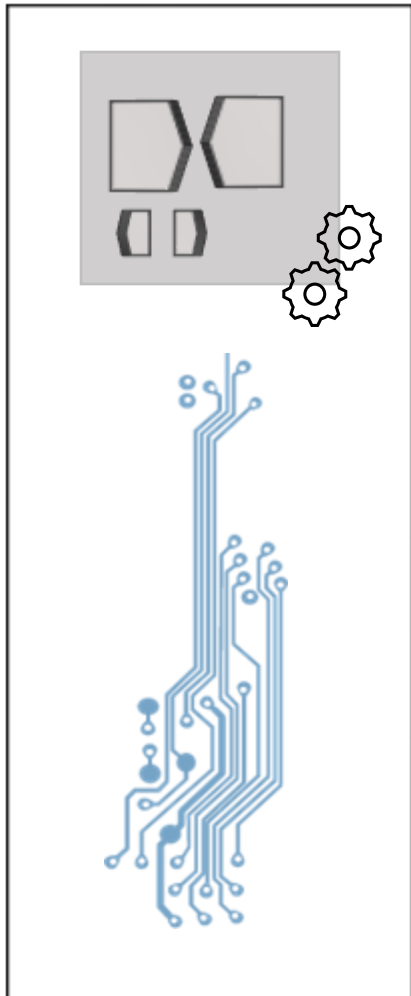
BOTTOM 377669-2.GBX

Calculate

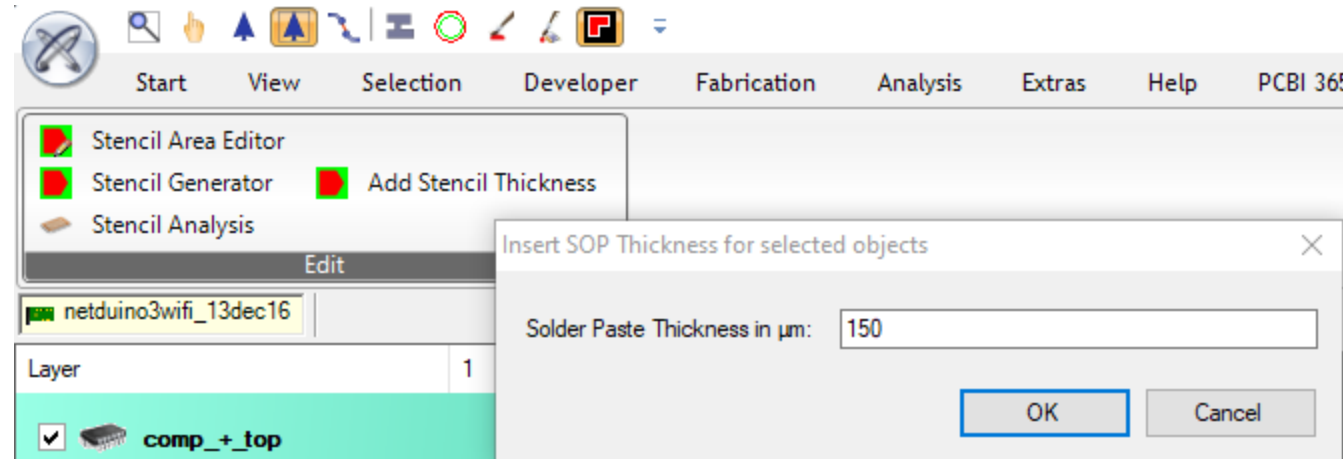
Export CSV

Close

# Stencil Wizard



## Global stencil thickness



You can set the thickness in the ODB++ attribute, the value is used in the SPI exports e.g. by Viscom to set different values for the paste thickness.

Note: If you do not save the zone values in the ODB attribute, they will not be recognized during export.



# Request Customized Functions

Get in touch,

[info@easylogix.de](mailto:info@easylogix.de)

Guenther Schindler

Tel. +49 941 568 136 26

## Useful Links:

PCB-Investigator  
[www.pcb-investigator.com](http://www.pcb-investigator.com)

PCBi-Physics  
[www.PCBi-Physics.com](http://www.PCBi-Physics.com)

Native Board Import (3D Interface to CATIA, SiemensNX, SolidWorks, SolidEdge)  
[www.sts-development.biz](http://www.sts-development.biz)

GerberLogix  
[www.gerberLogix.com](http://www.gerberLogix.com)

Online Gerber Viewer  
[www.Gerber-Viewer.com](http://www.Gerber-Viewer.com)

Software Development, CAD Converter, data connection  
[www.easyLogix.de](http://www.easyLogix.de)

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