CAD/CAM
for electronics

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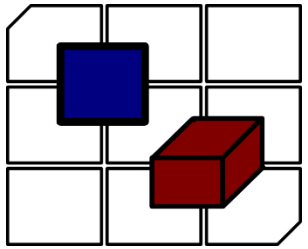
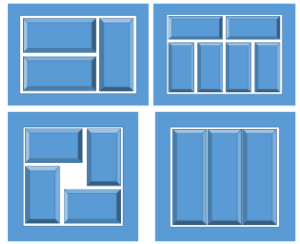
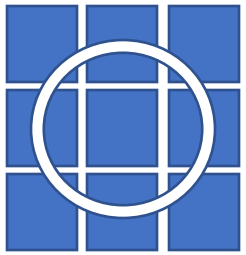
PCB-Investigator


PCB-I-Online


Native Board Import


Panel Optimizer


PCB-I-Physics


PLM

High Quality Stencil Preparation

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01/2023

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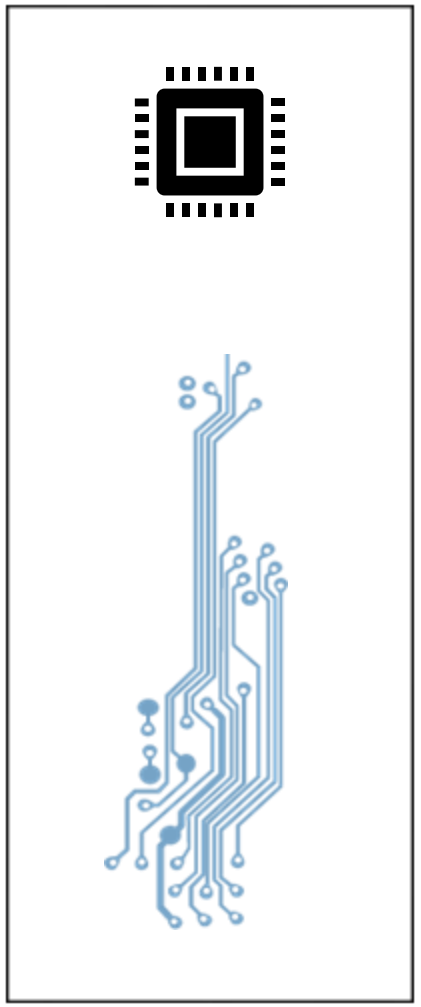
Product Categories



- **PCB Assembly**
- **PCB Manufacturing**
- **PCB Testing**
- **Material Libraries**
- **Component Libraries**
- **Package Libraries**
- **EMS Manufacturing**
- **Layout Design**
- **Thermal & Current Simulation**
- **Digital Twin**
- **Design Review**
- **Equipment Integration**
  - AOI, Solder Machine, Boundary Scan, Direct Imaging

Advanced Stencil Preparation

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Increase in Efficiency and Productivity

PCB-Investigator automates data preparation while allowing the flexibility customers needs.
Takin care of all different types of stencils and components.

Standard Stencil design / Step-Stencil Technologies

Train your CAD System for best results
Use knowledge getting from components
Adding the experience from internal production
Set up a looped process to learn with each product

IPC-7525A
Stencil Design Guidelines

- **Electroforming**
- **Laser Cutting**
- **Chemical Etching**

- **Stainless Steel SMT Stencils**
- **Mylar and Kapton SMT Stencils**

Advanced Stencil Preparation

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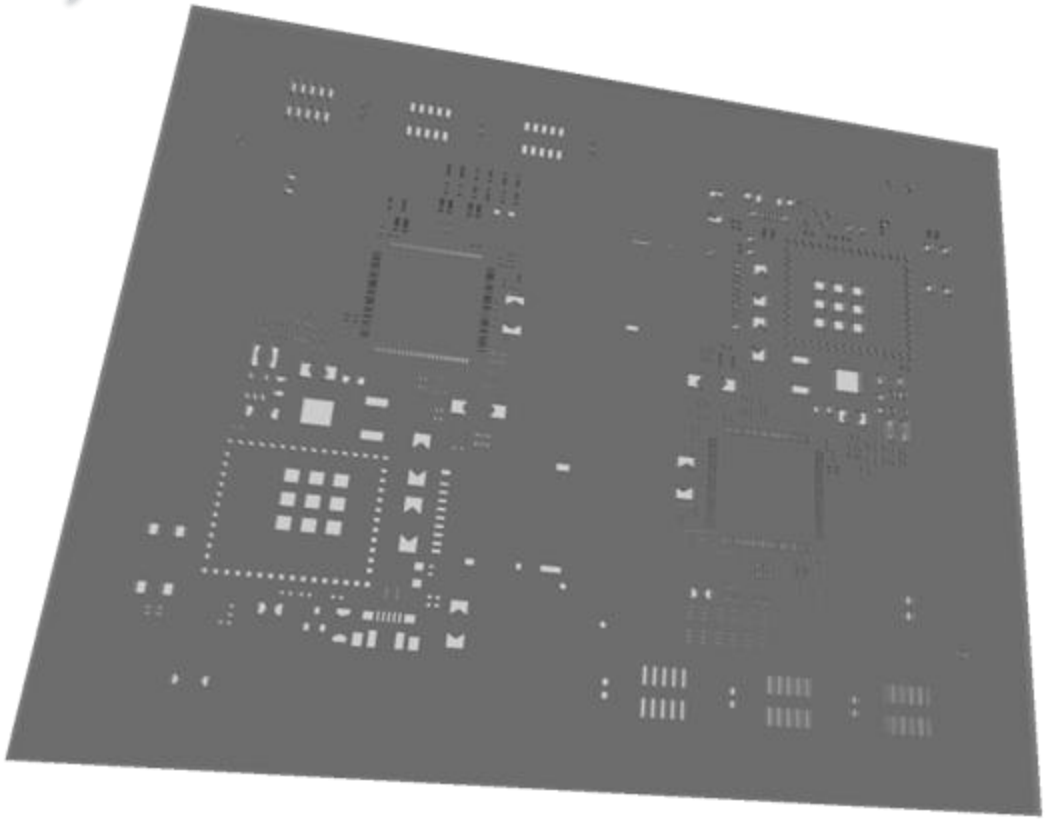
One of the features of PCB-Investigator is its ability to handle all different types of stencils and components. This includes standard stencil design and step-stencil technologies, as well as stencils made using electroforming, laser cutting, chemical etching, and other techniques. PCB-Investigator can also support different types of stencil materials.

In addition to its automation capabilities, PCB-Investigator also offers flexibility to meet the specific needs of customers. This includes the ability to train the CAD system for optimal results, use knowledge gained from components and internal production experience, and set up a looped process to learn with each product. By using PCB-Investigator, customers can streamline their data preparation process and improve their efficiency and productivity in PCB manufacturing.

Advanced Stencil Preparation

Area Editor
Stencil Generator
Stencil Analysis



Suitable for both standard and STEP stencils.

Switching from predefined to rule-based creation improves the automation process, making it more reliable and independent. This approach also puts the production technology in the forefront, ensuring that the process is tailored to the specific requirements of the application..

Package Types

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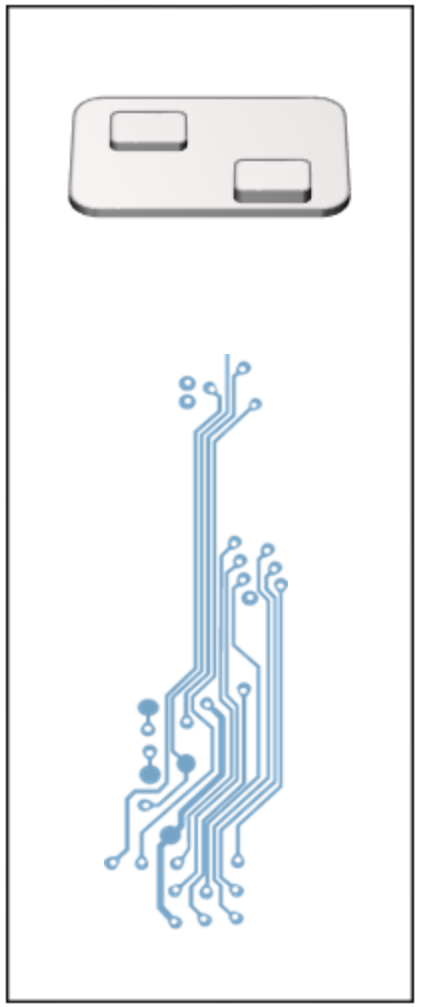
Assign the right optimization to each package

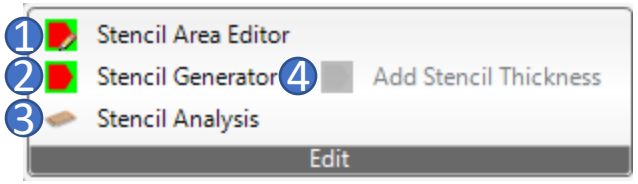
- QFN - quad flat pack
- PQFN - power quad flat-pack, no-leads, with exposed die-pad[s] for heat sinking.
- BGA - ball grid array
- CGA - column grid array
- CCGA - ceramic column grid array
- BGA - micro-BGA, with ball spacing less than 1mm.
- COB - chip-on-board
- COF - chip-on-flex
- COG - chip-on-glass
- SOIC Small outline integrated circuit
- SOP Small outline package
- PLCC Plastic leaded chip carrier
- TSOP Thin small outline package
- SSOP Shrink small outline package
- TSSOP Thin shrink small outline package
- QSOP Quarter-size small outline package
- VSOP Very small outline package
- LQFP Low profile quad flat pack
- PQFP Plastic quad flat pack
- CQFP Ceramic quad flat pack
- TQFP Thin quad flat pack
- MLP – Lead-frame package
- MQFP - Metric Quad Flat Pack
- CSP – Chip Scale Package

Using PCB-Investigator, customers can automate the stencil preparation process and streamline their PCB manufacturing workflow. The tool can help to ensure that the correct stencils are created for the package types being used, improving efficiency and reducing the risk of errors.

Stencil Wizard



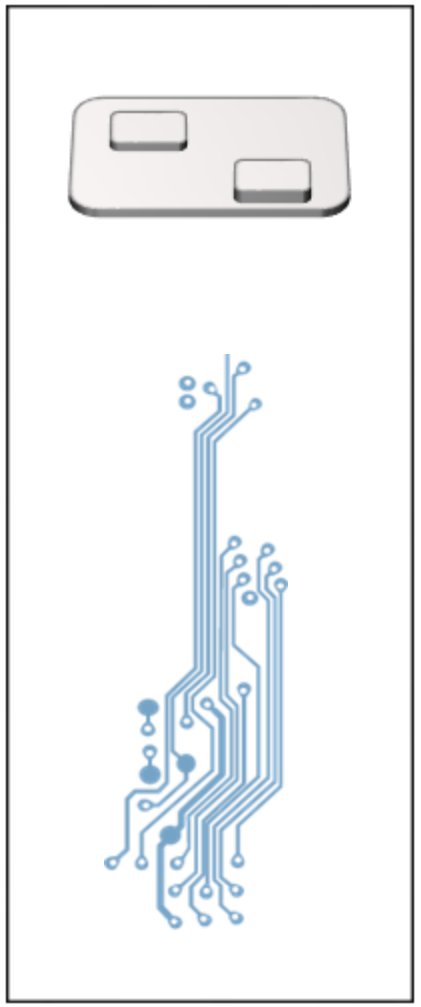
Advanced rule-based stencil generation taking component information into account



To create high-quality SMT pads for your stencil, the following steps should be taken:

-Create all necessary patchwork and steps for your stencil
-Use all relevant rules to create the SMT pads
-Ensure that the stencil conforms to IPC standards
-Set the overall thickness of the stencil to the appropriate level for the specific application.

Stencil Wizard



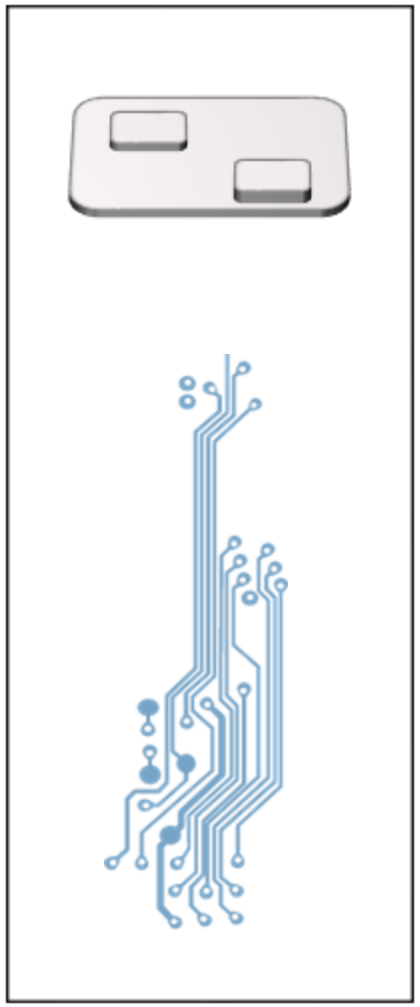
Advanced rule-based stencil generation taking component information into account

PCB-Investigator is used to create patch work and steps for stencils. PCBI can be configured to use a variety of rules to create high quality SMT pads, ensuring that the stencils produced meet industry standards and are suitable for use in PCB manufacturing.
In addition to creating the patch work and steps, PCB-Investigator can also be used to check the stencil against IPC (International Electrotechnical Commission) standards.

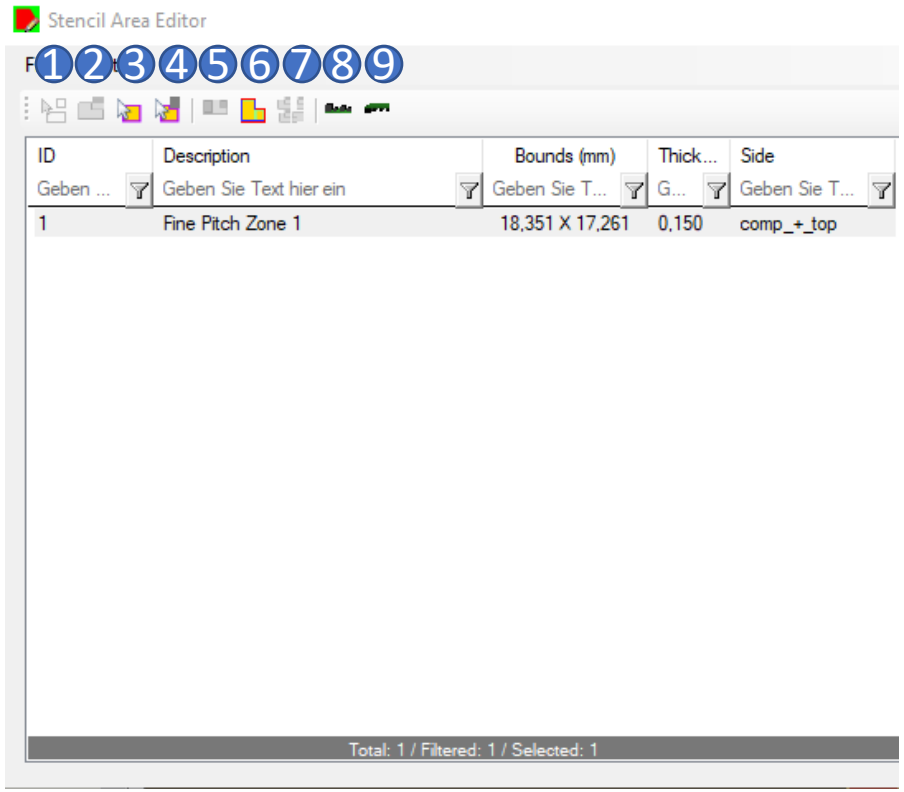
This can ensure that the stencil meets the necessary quality and performance requirements for your project.

PCB-Investigator can set the overall thickness of the stencil, ensuring that it is suitable for use with the particular manufacturing process and equipment being used. By using PCB-Investigator, customers can streamline their stencil preparation process and improve the efficiency and quality of their PCB manufacturing operations.

Stencil Wizard



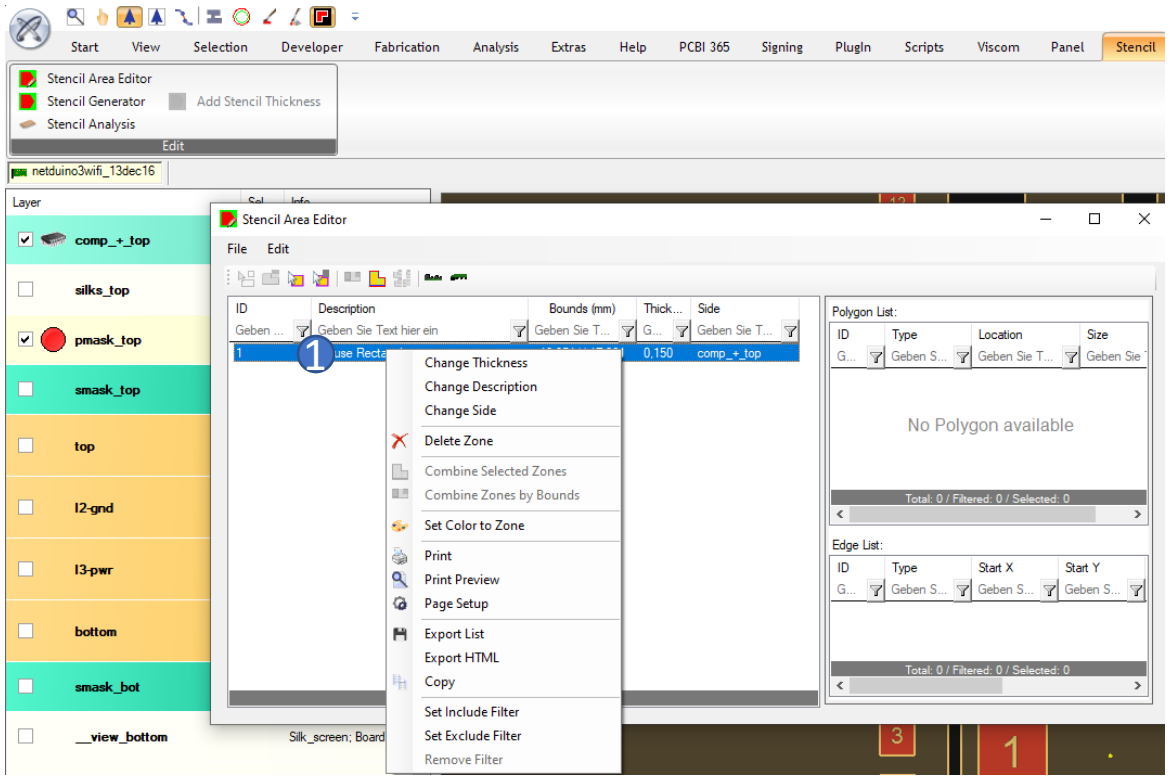
Stencil Area Editor operations



1. Add selection as zone
2. Set Area
3. Add zone by rectangle
4. Add zone by rectangle with cutouts
5. Combine selection
6. Add zone rectangle
7. Combine zones overlapping
8. Switch to Top View
9. Switch to Bot View

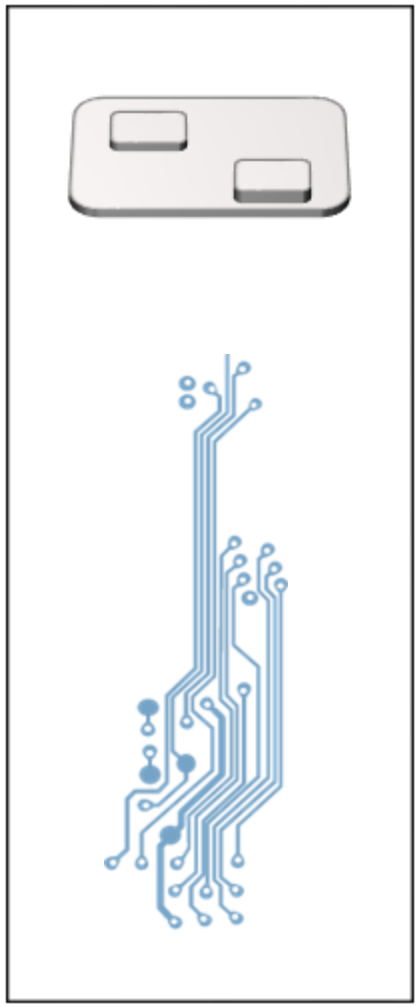
Stencil Area Editor

Edit base settings for each area

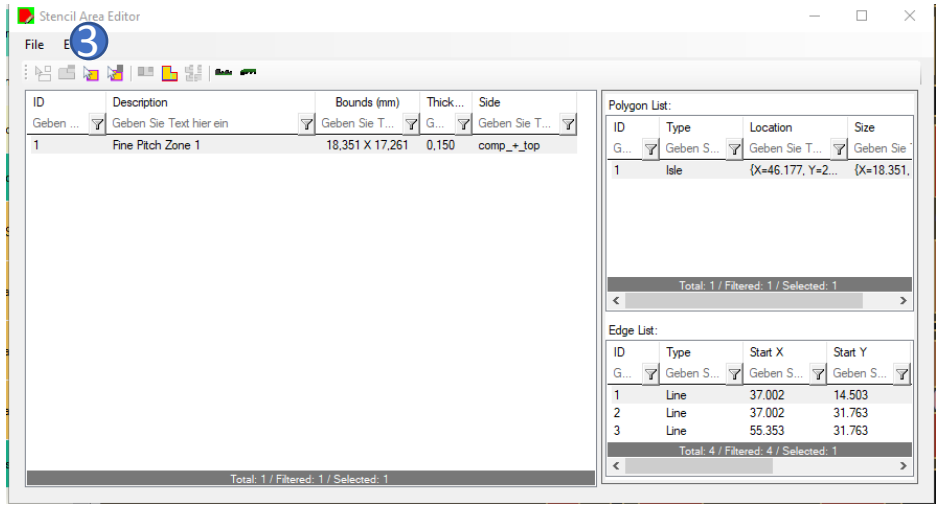


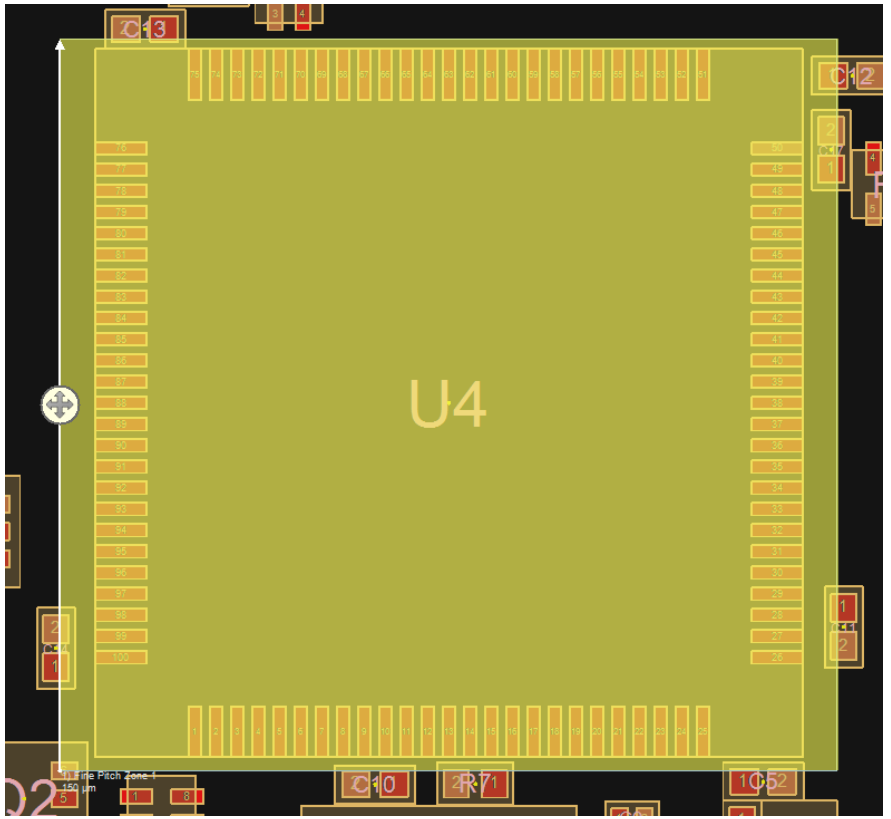
1. Context menu

Stencil Area Editor



Edit the shape



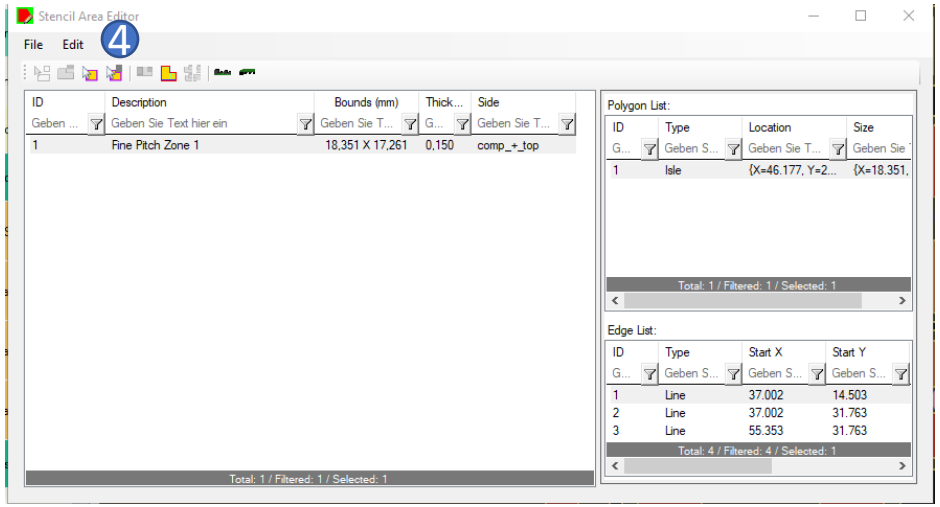


3. Add a new zone by drawing a rectangle

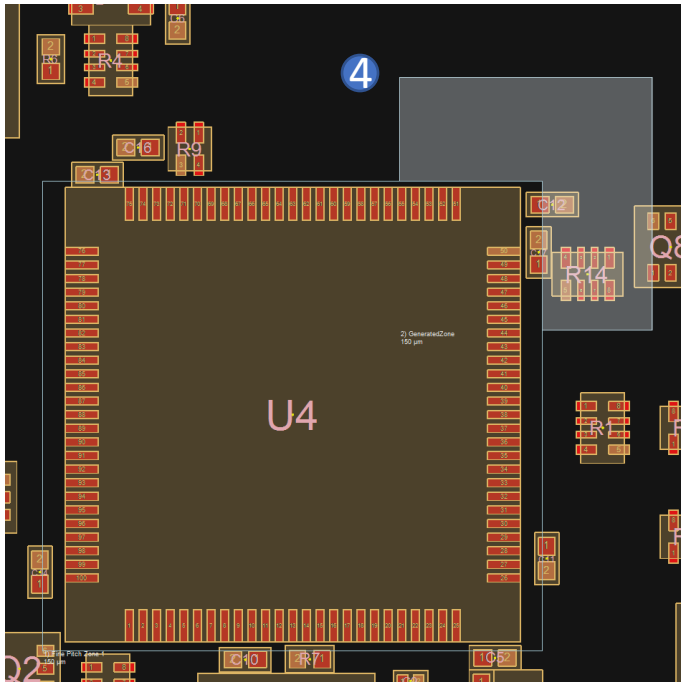
Note: For high quality, it is recommended not to cut pin pads. You can combine areas e.g. from different parts to get ideal areas.

Stencil Area Editor

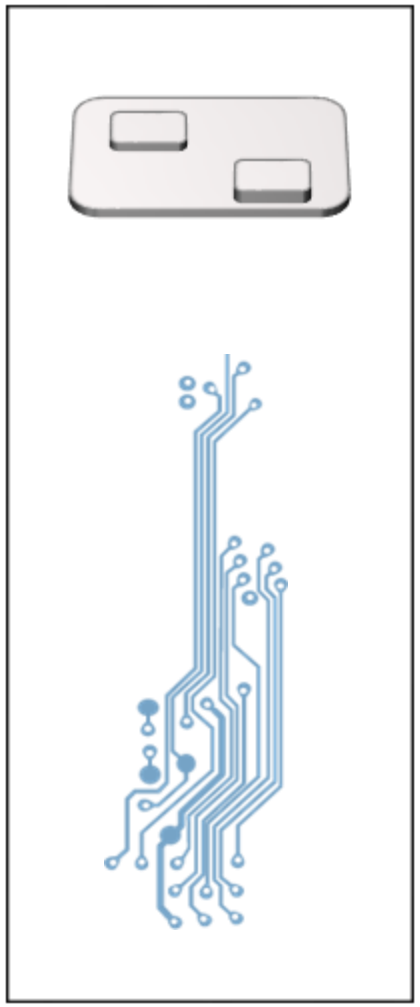
Zone function



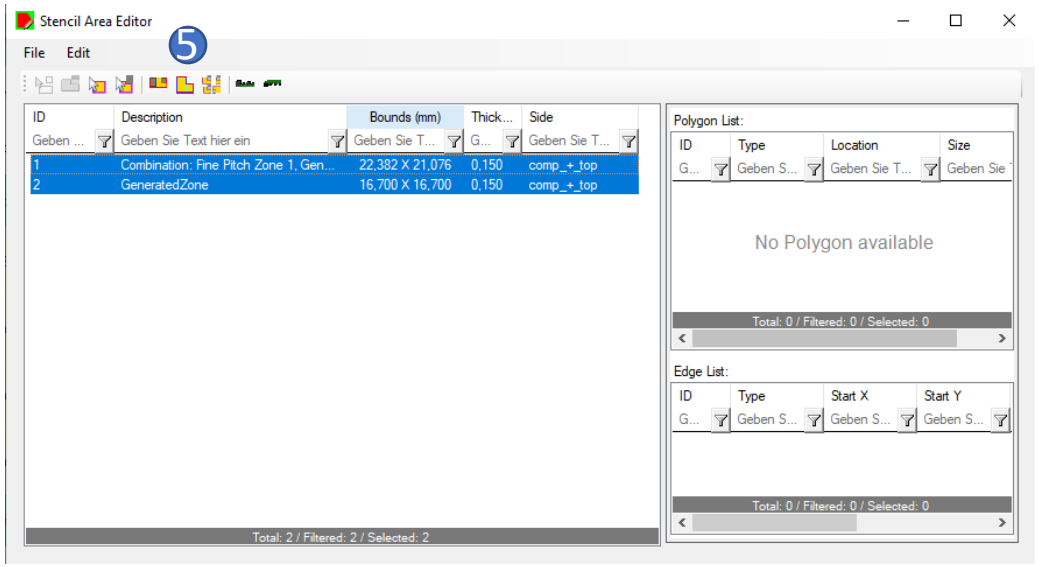
4. Add a new zone with cutting out a previous zone by drawing a rectangle



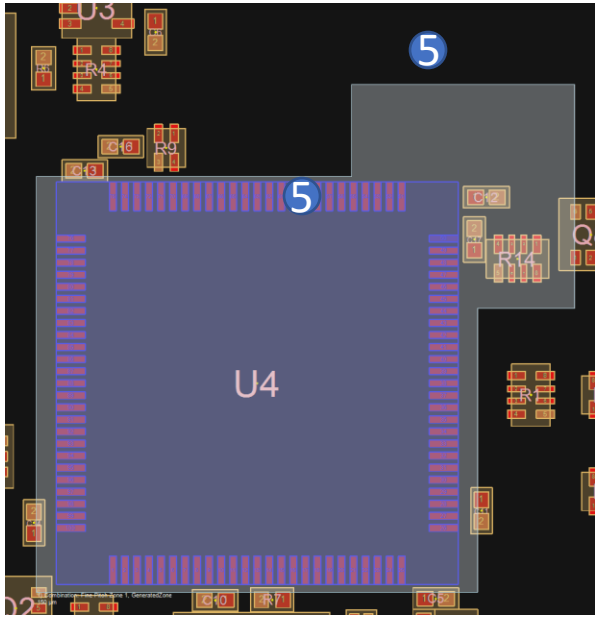
Stencil Area Editor



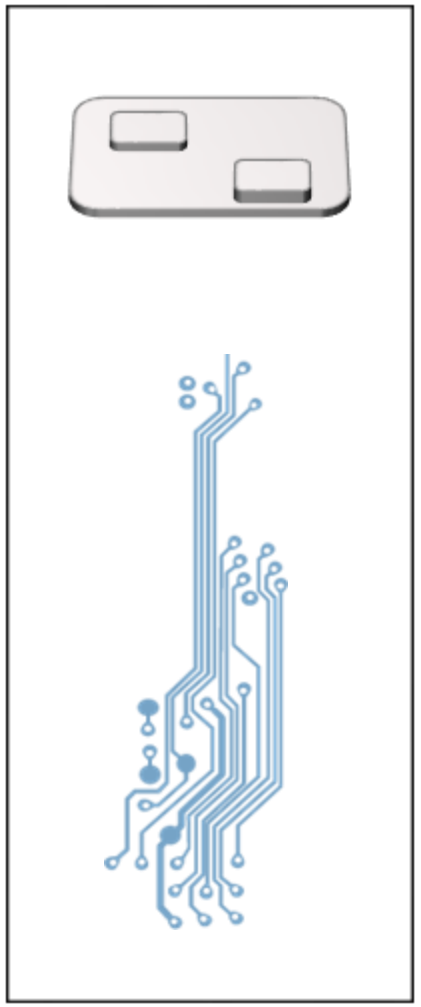
Zone function



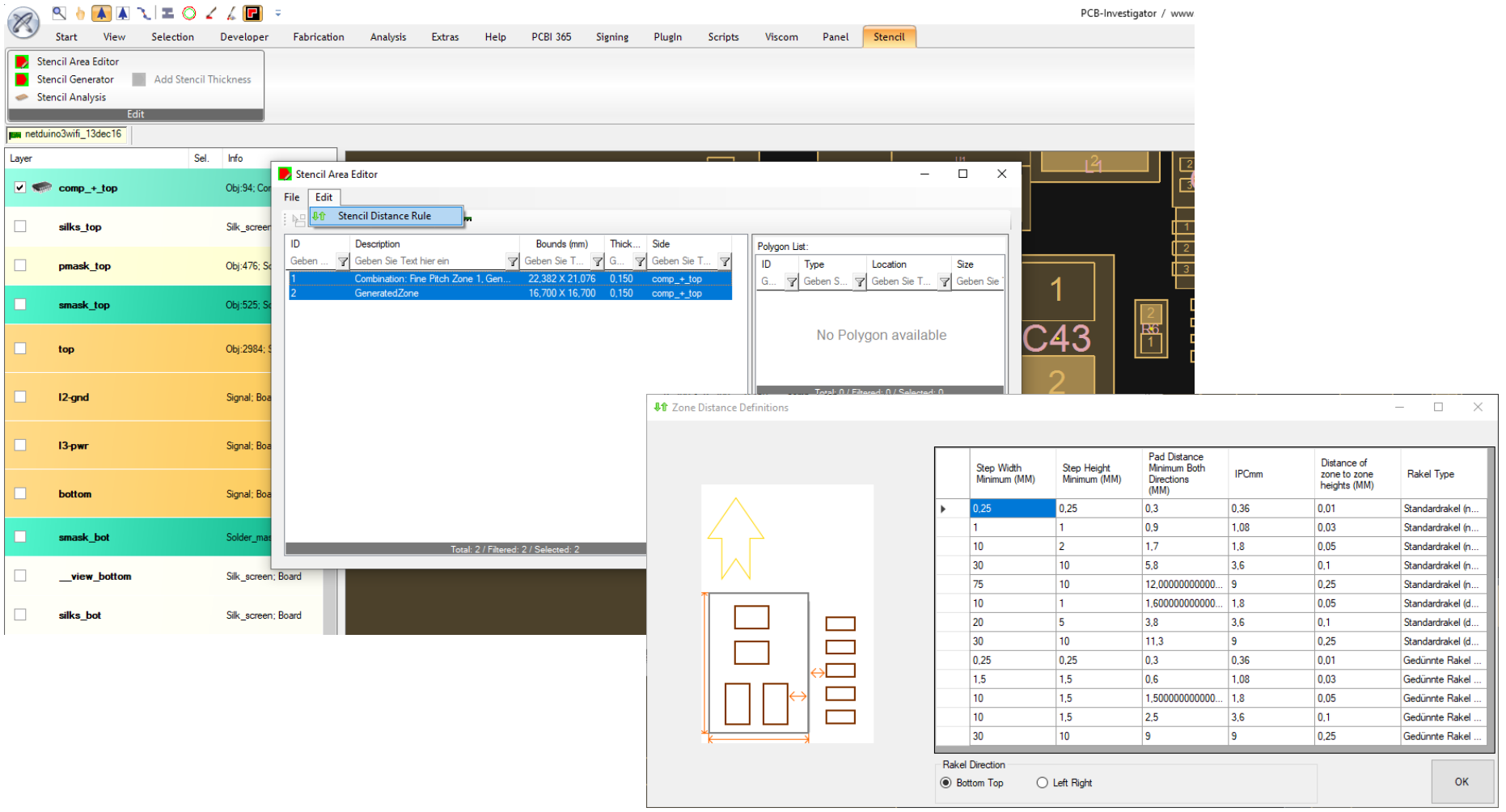
5. Combine different zones to one zone



Stencil Wizard

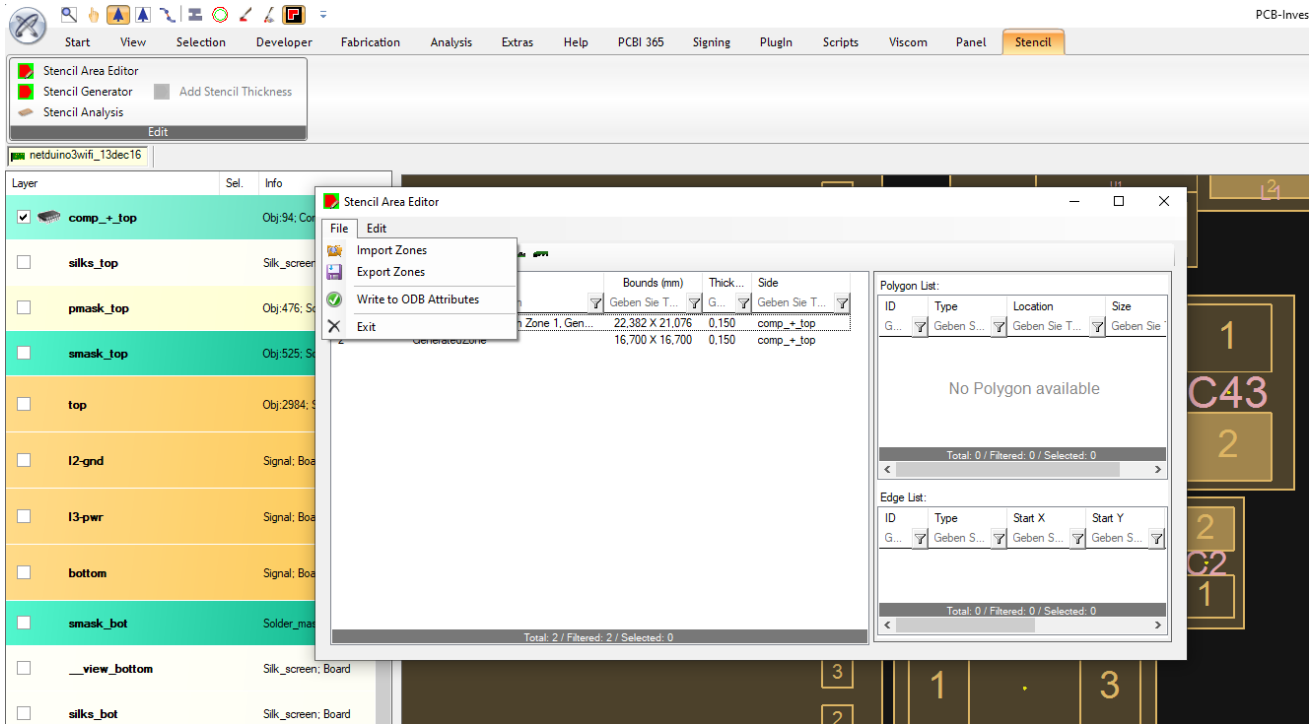


Clearance analysis



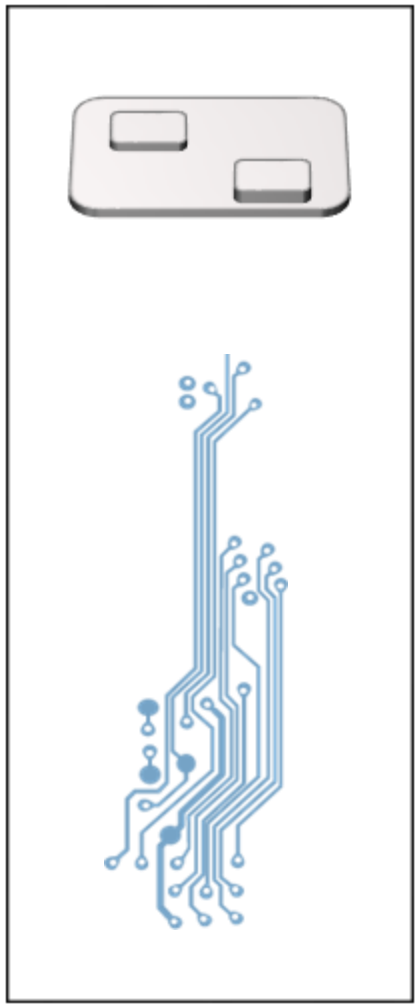
Stencil Area Editor

Manage zone settings



Zone settings can be saved in ODB attributes, exported as xml and imported from xml.

Stencil Area Editor

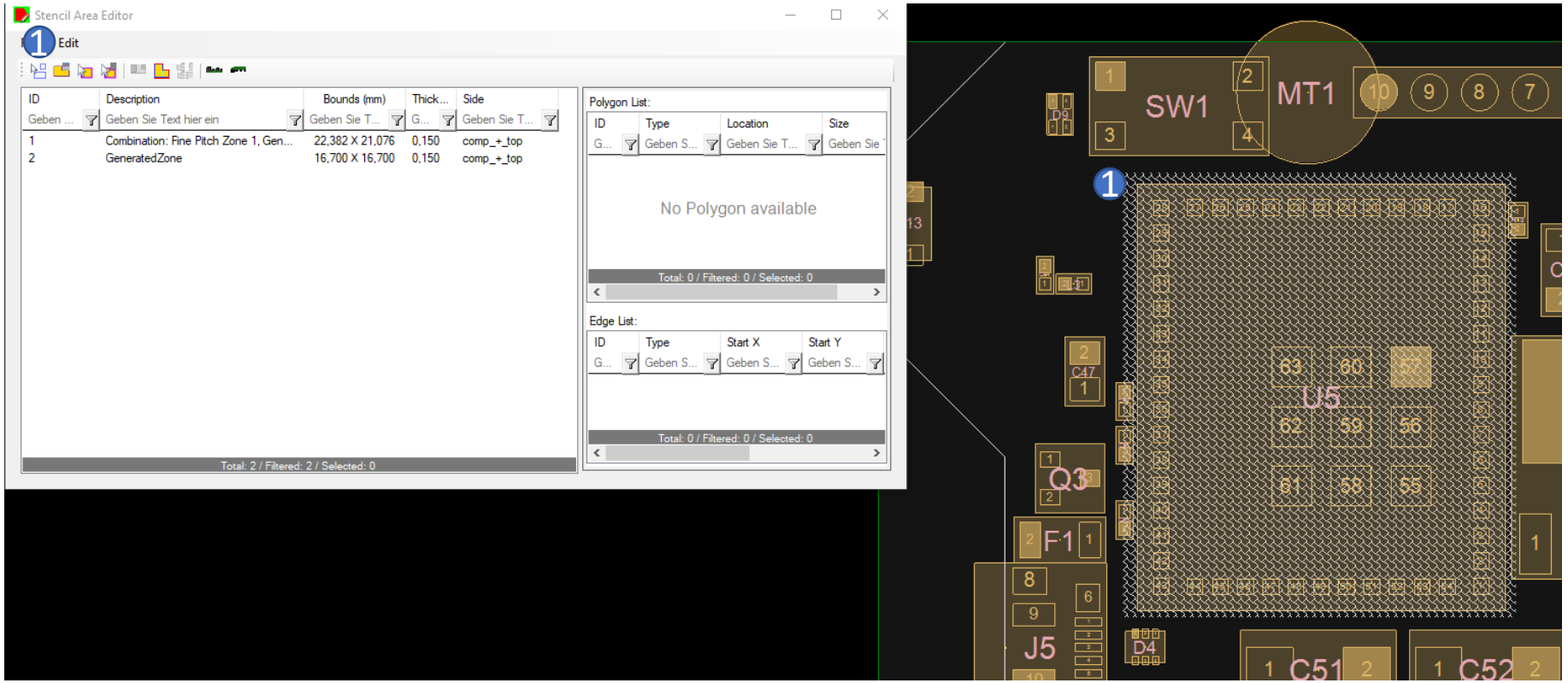


Add zones by predefined drawings

1.Increased flexibility: A step stencil allows for different paste deposition levels in different areas, which can be useful for specific applications.
2.Improved accuracy: The different thickness levels in a step stencil can provide more precise and accurate paste transfer, as the aperture walls are closer to the pads in some areas.
3.Reduced paste bridging: The different thickness levels in a step stencil can reduce the risk of paste bridging between apertures, which can lead to better yields and improved overall quality of the soldered joints.
4.Reduced costs: A step stencil allows for more efficient use of paste, which can lead to reduced costs for the soldering process.
5.Increased process control: By adjusting the thickness of the stencil at different areas, it allows better control of the paste depositon, which can have a positive impact on the final product quality.

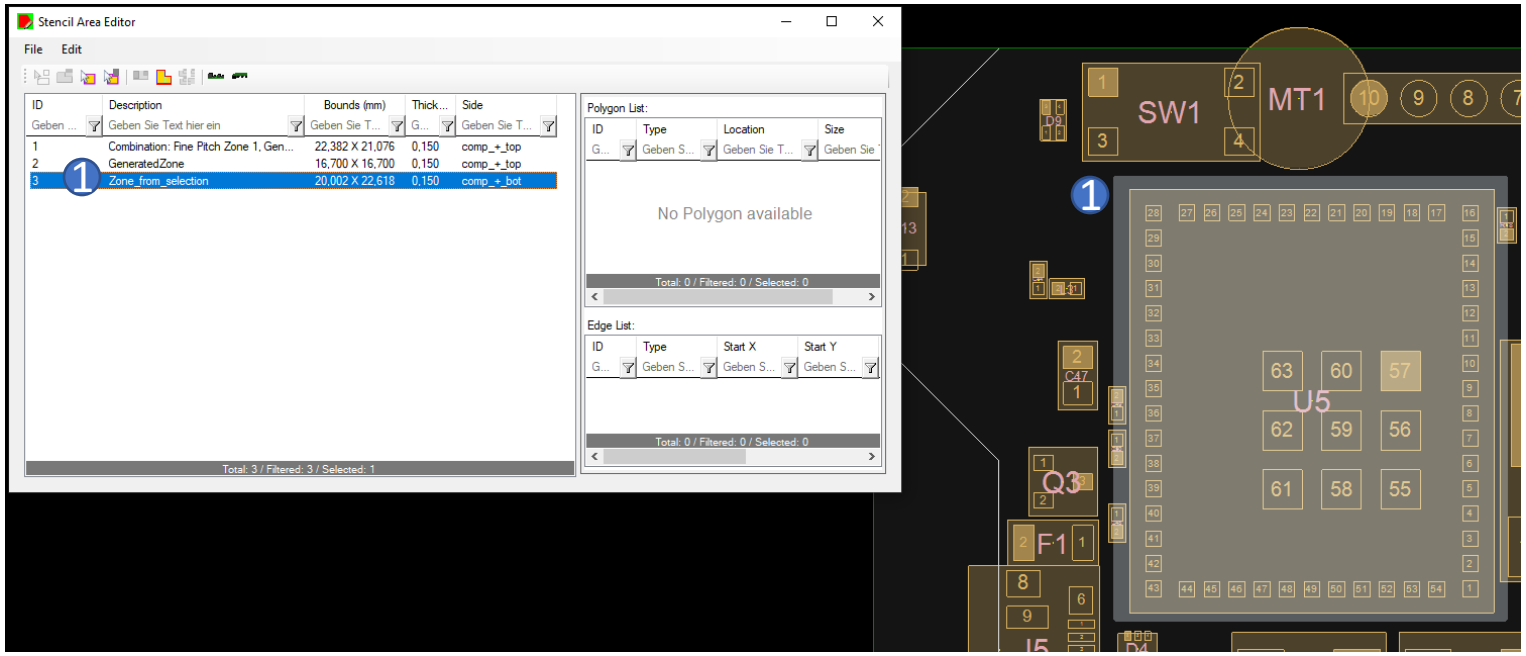
Stencil Area Editor

Add zones by predefined drawings



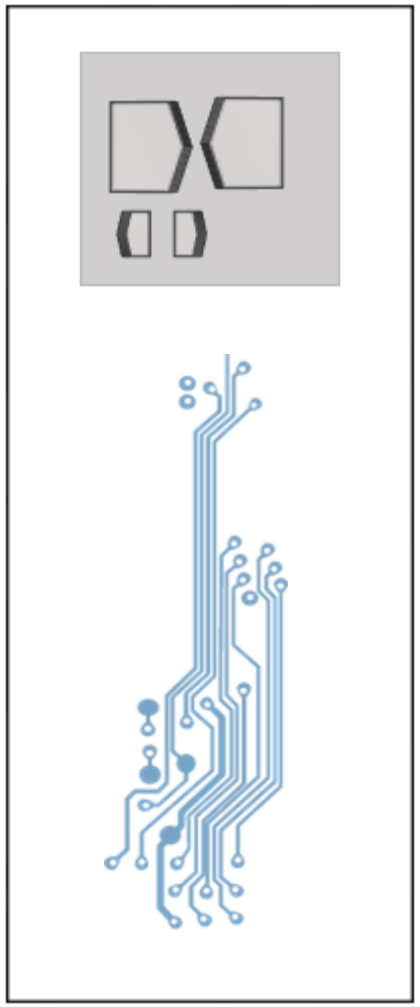
Stencil Area Editor

Add zones by predefined drawings

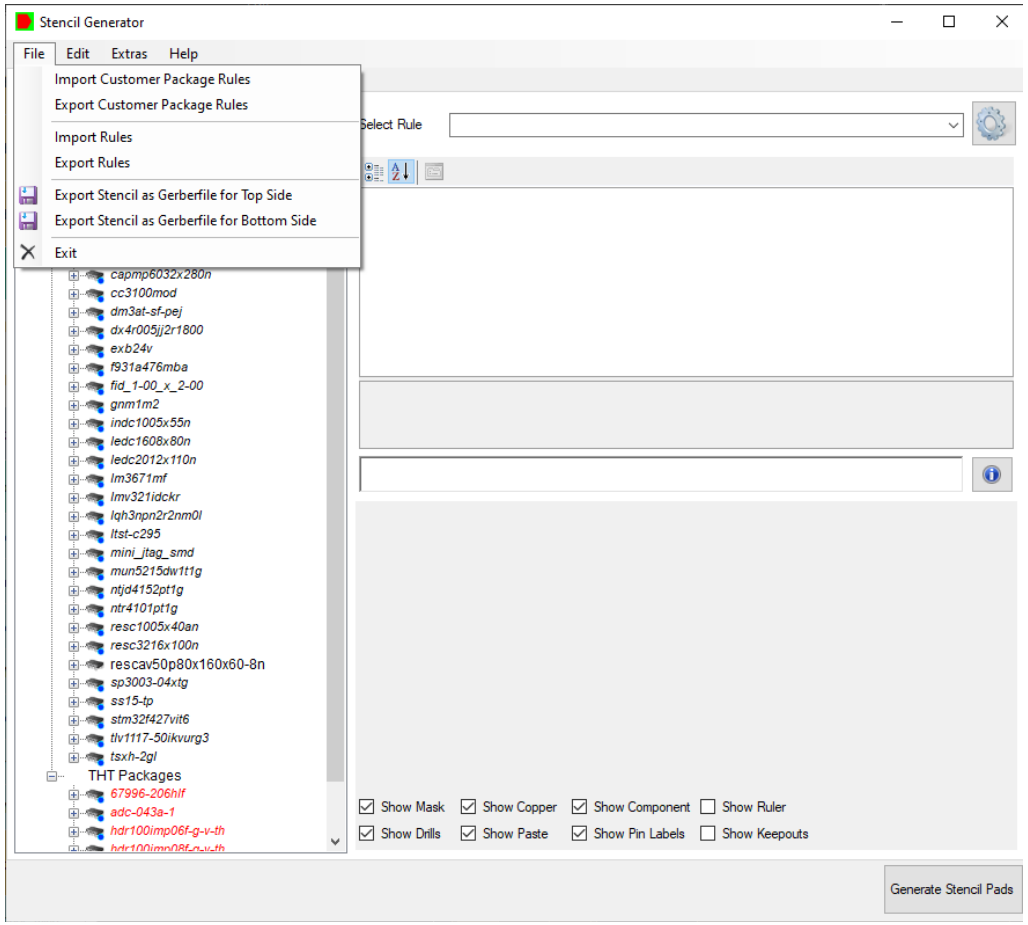


Improved accuracy: Smaller thickness stencils can provide more precise and accurate paste transfer, as the aperture walls are closer to the pads.
Better paste release: The thinner stencils can lead to better release of the paste from the apertures, resulting in more consistent and reliable paste deposition.
Reduced paste bridging: Thinner stencils can reduce the risk of paste bridging between apertures, which can lead to better yields and improved overall quality of the soldered joints.
Reduced costs: Thin stencils require less material, which can lead to reduced manufacturing costs.
Increased flexibility: Thin stencils can be more flexible, which can be useful in applications where the stencil needs to conform to irregular or curved surfaces.

Stencil Generator



Main setup for paste pad creation



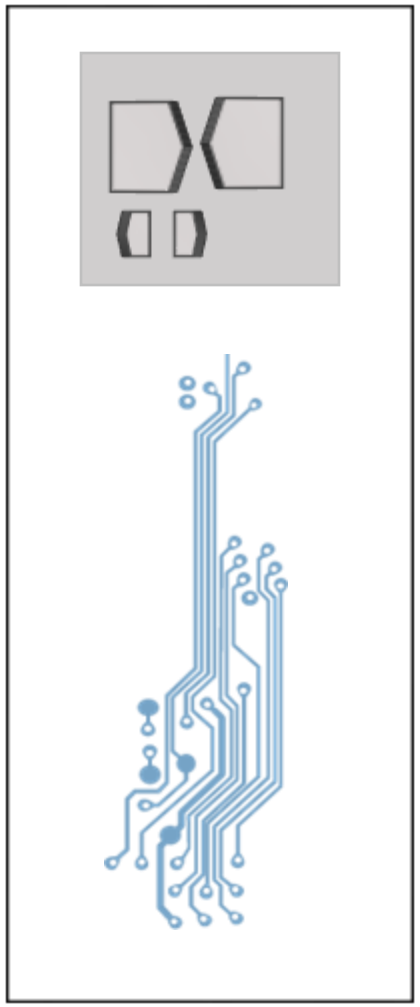
The Stencil Generator uses all zones defined by the Stencil Area Editor. If there are no zones the outline will be used as main zone.

Use default rules for your company.

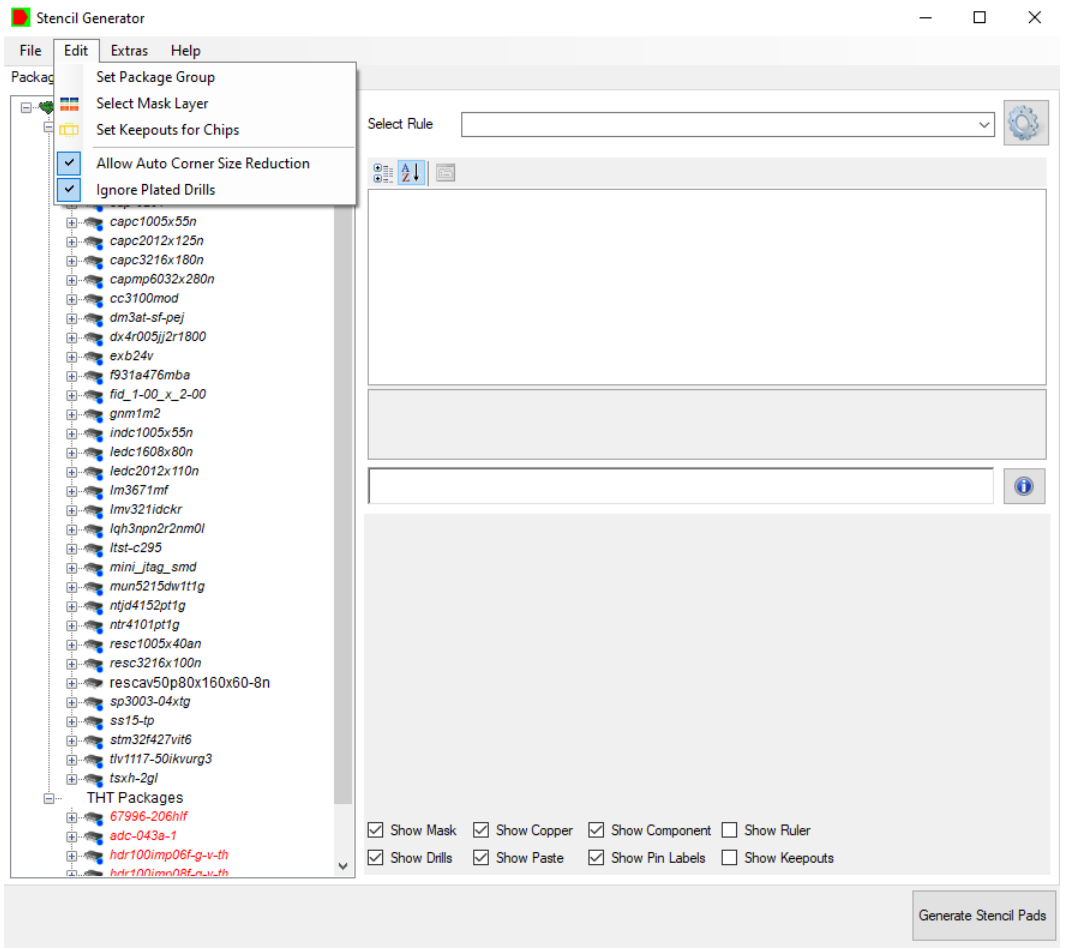
Setting a package group, enables the Wizard to set the rules regarding it. SOICs, Chips, BGAs and any definition needed.

The Wizard is delivered we predefined settings. To adjust all data preparation to your product you can setup own data preparation Scripts to adjust to your equipment.

Stencil Generator



Build in automation support



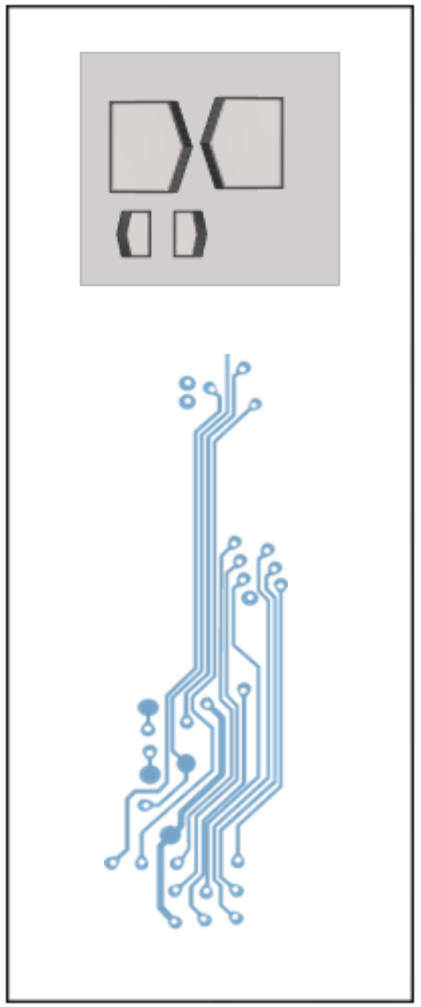
Set Package Group is only necessary if your data don't contain a proper information. Customers with EPL ("Easylogix Part Library") can resolve trusted data from EPL.

The Wizard also process layouts with multiple mask layers in the stack-up.

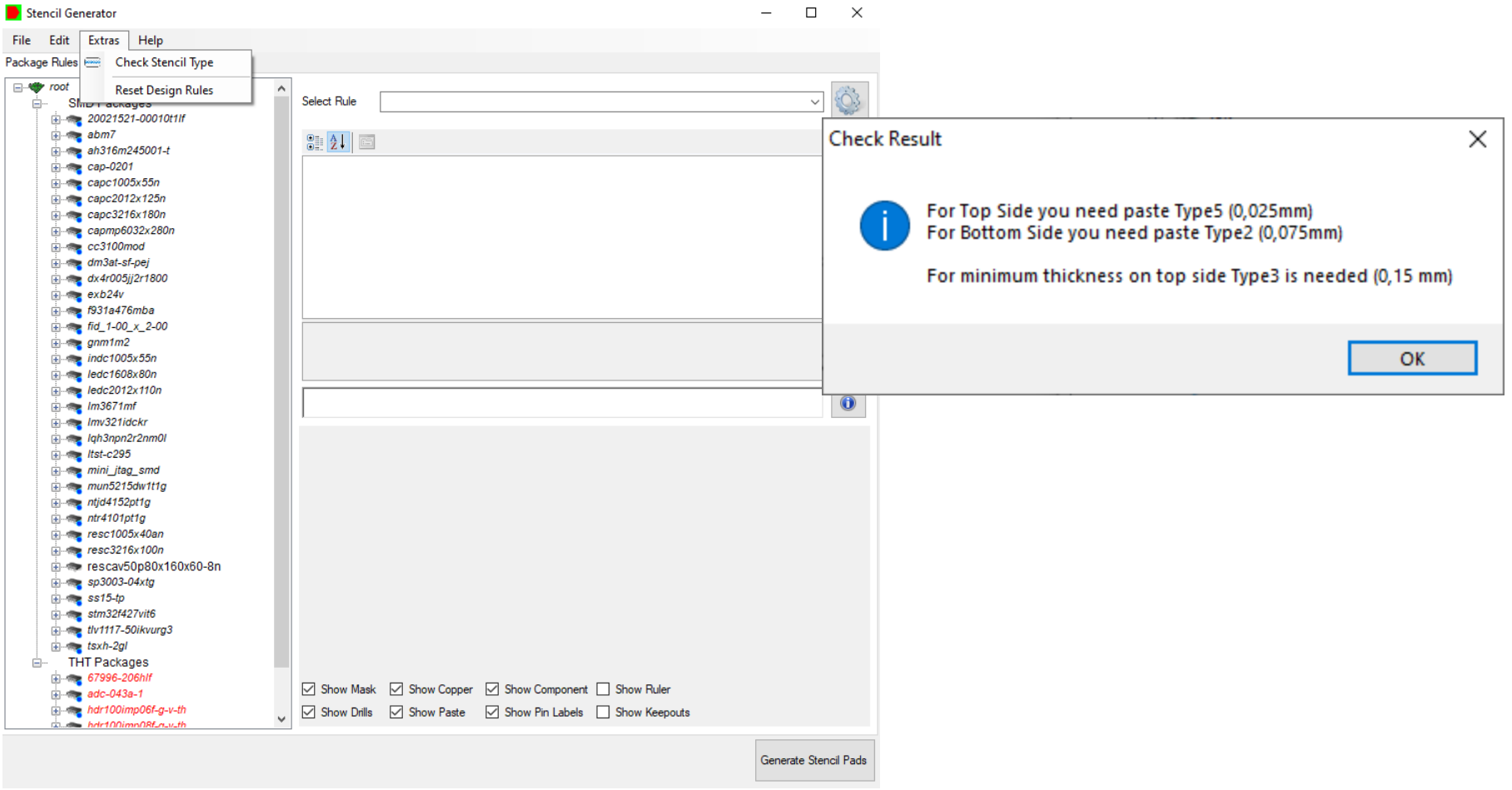
Set "Keepouts for Chips" is only available if you have MPN packaged defined. It will handle the usable area for you.

You also can set plugged drills as free usable area.

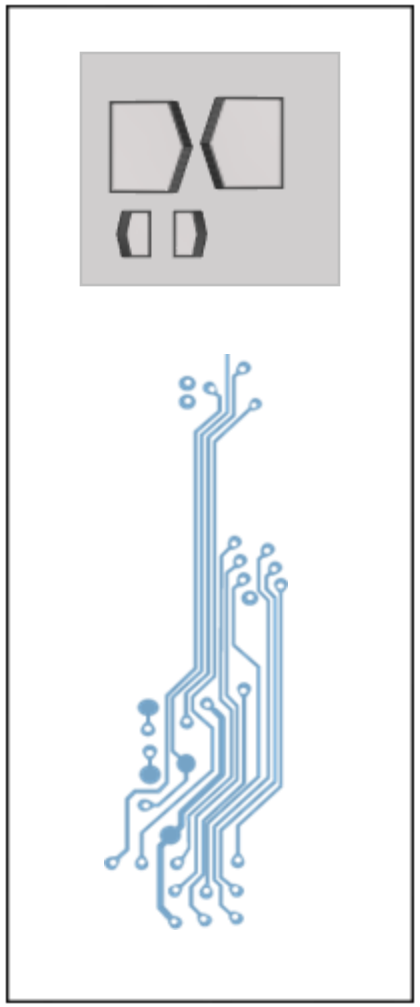
Stencil Generator



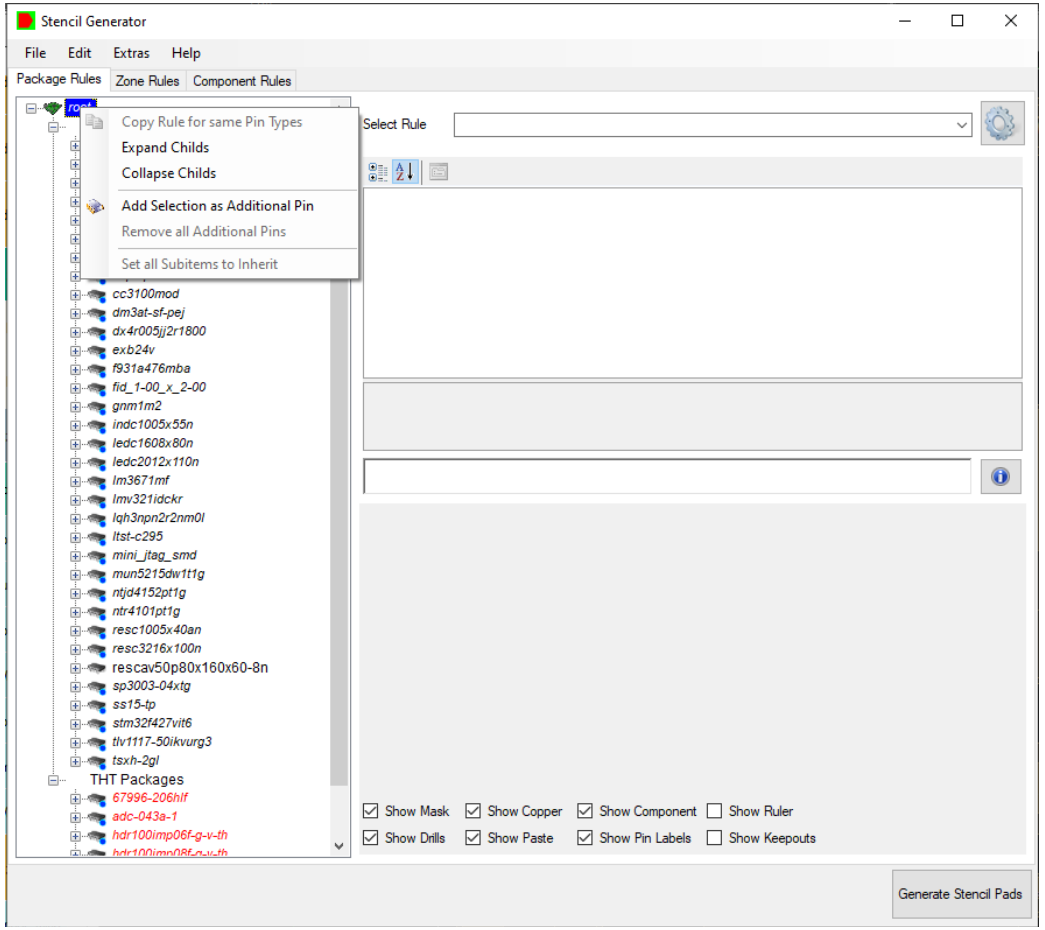
Check stencil by using current rules



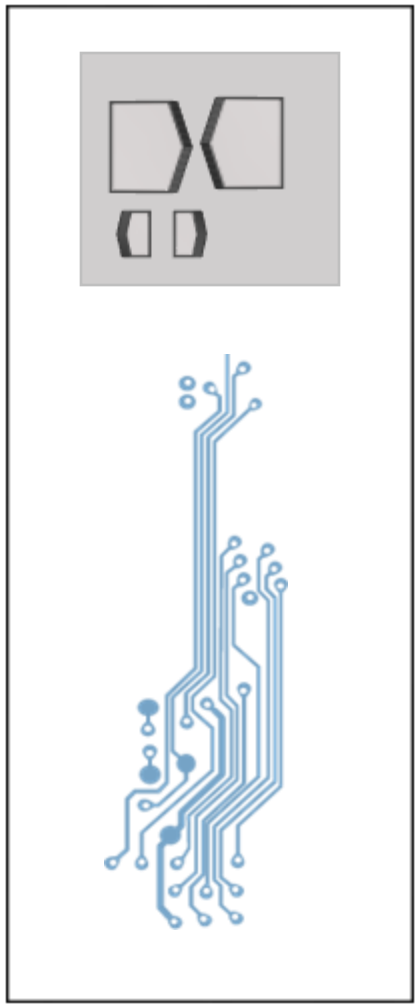
Stencil Generator



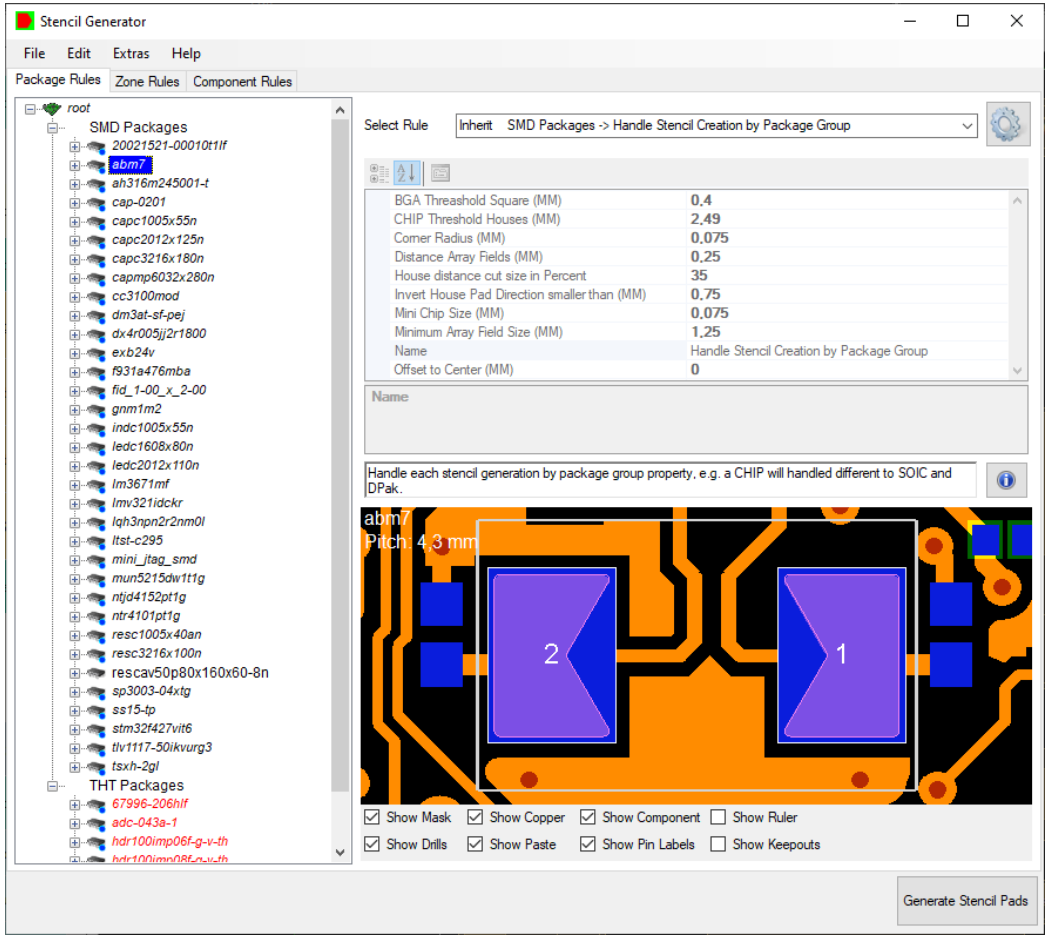
Crate stencil pin by any drawing



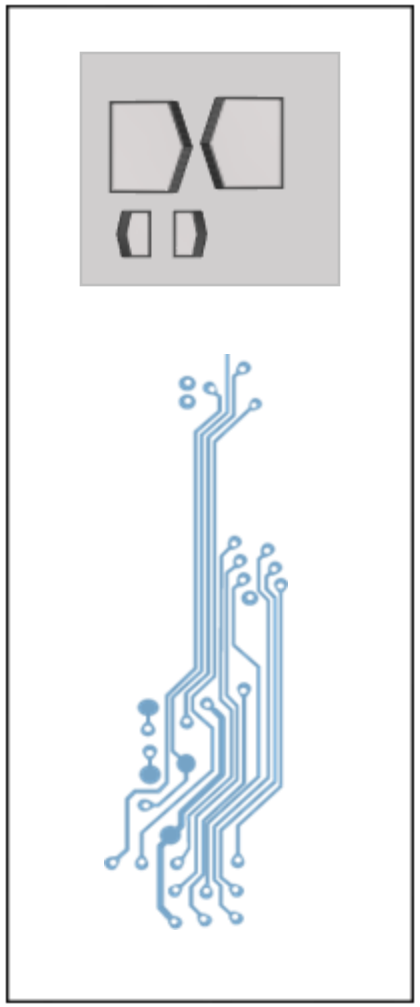
Stencil Generator



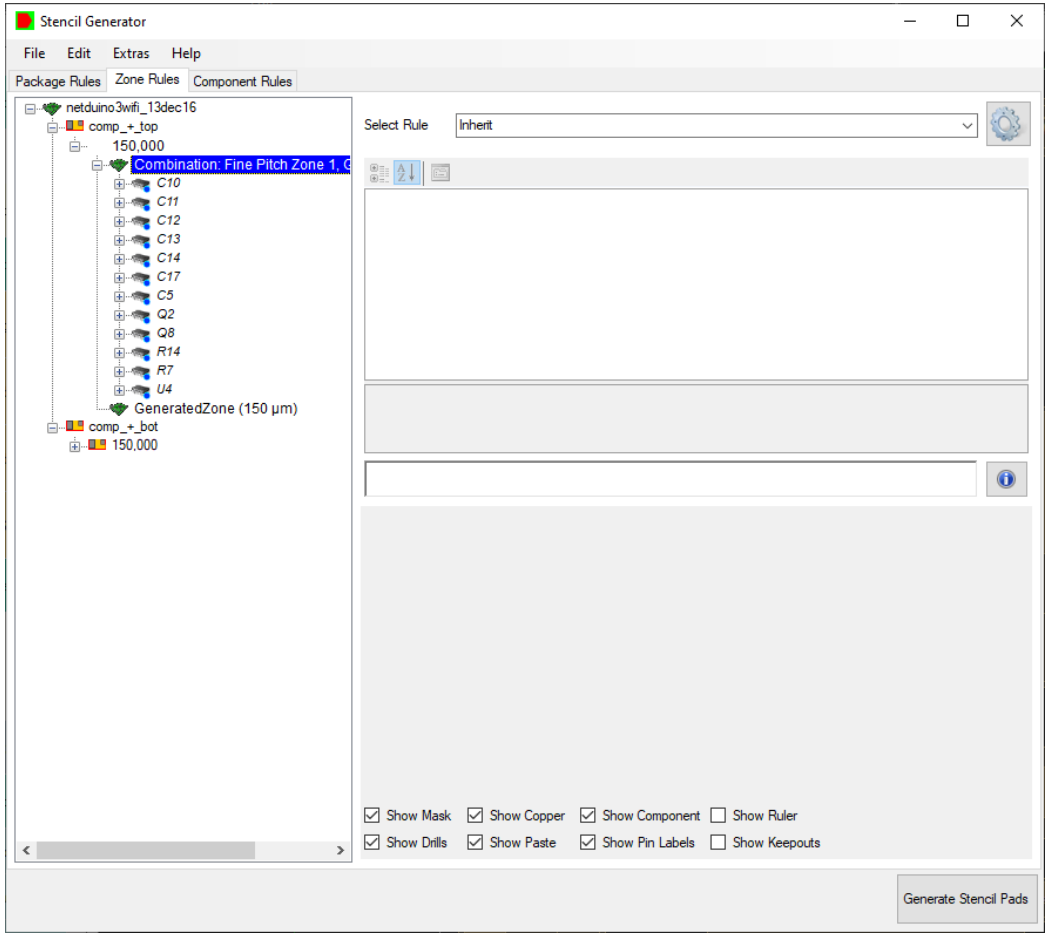
Rule preview



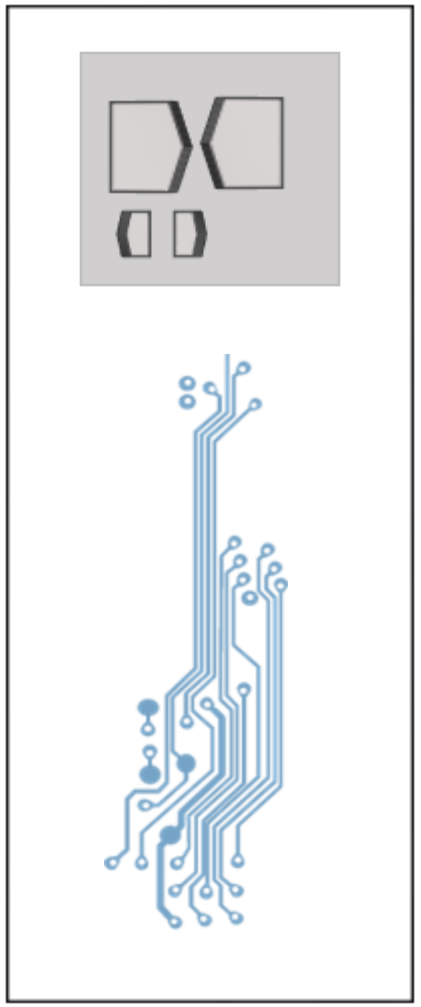
Stencil Generator



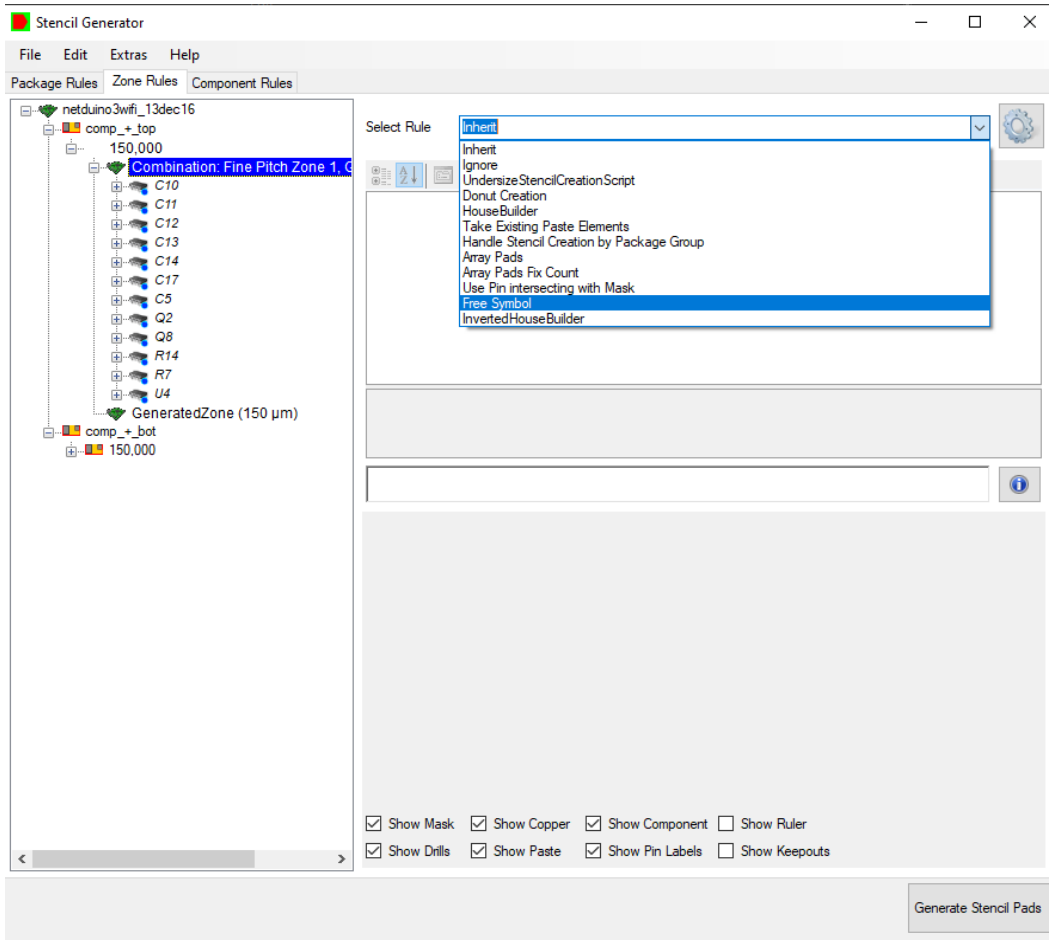
Set extra rules for components in defined zones



Stencil Generator



Set extra rules for components in defined zones



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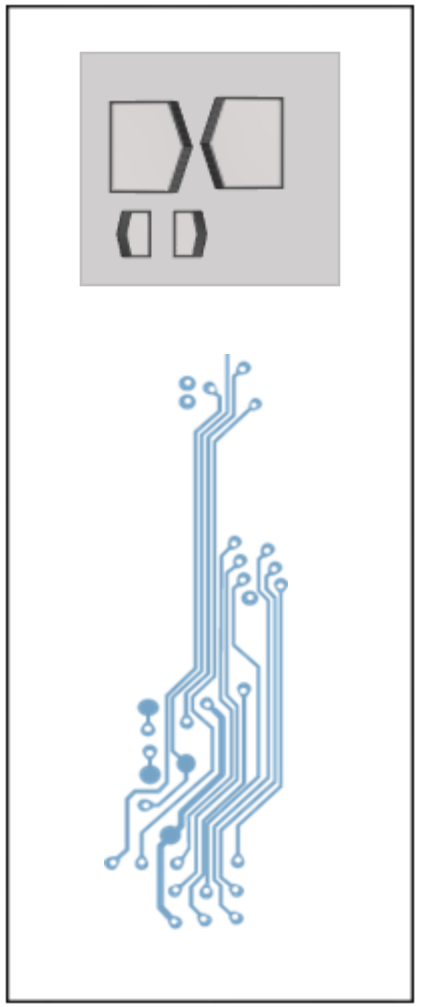

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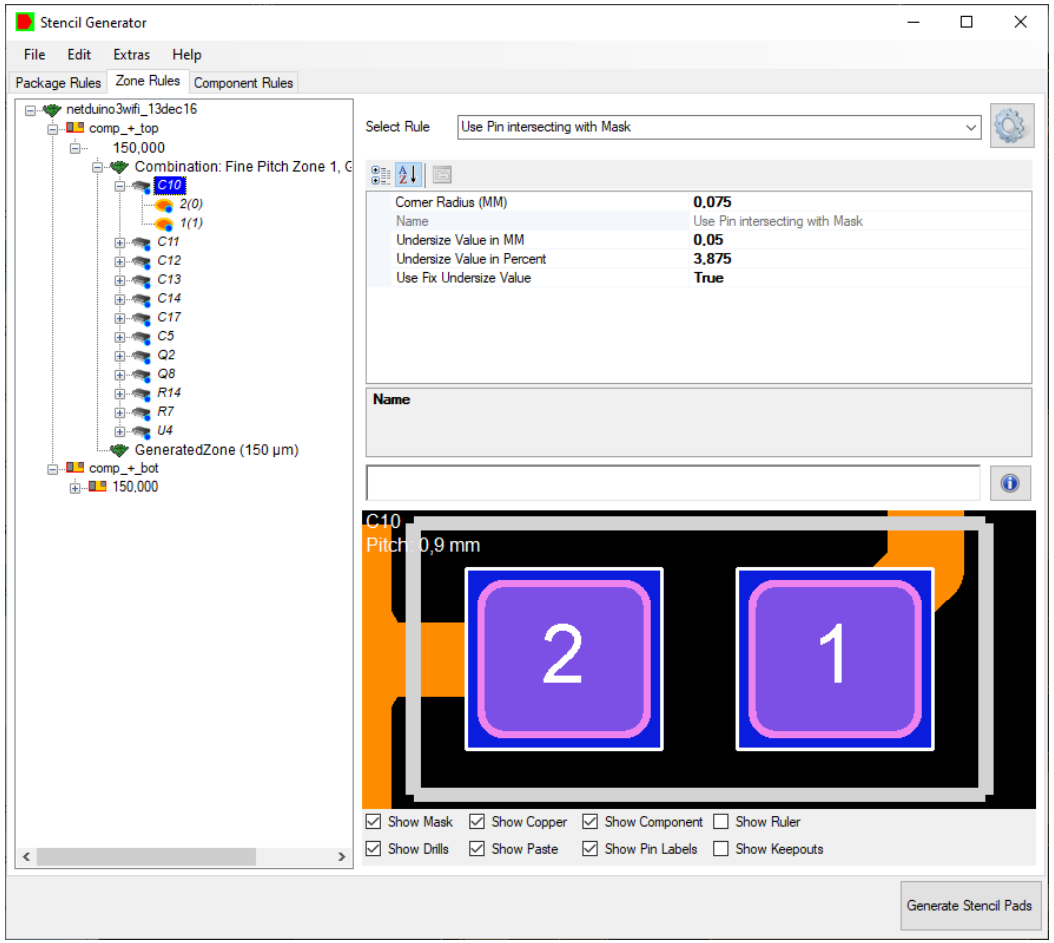
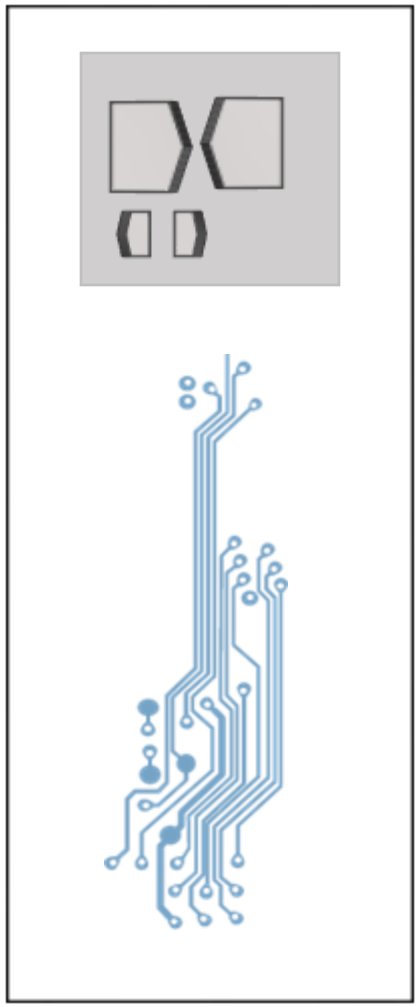
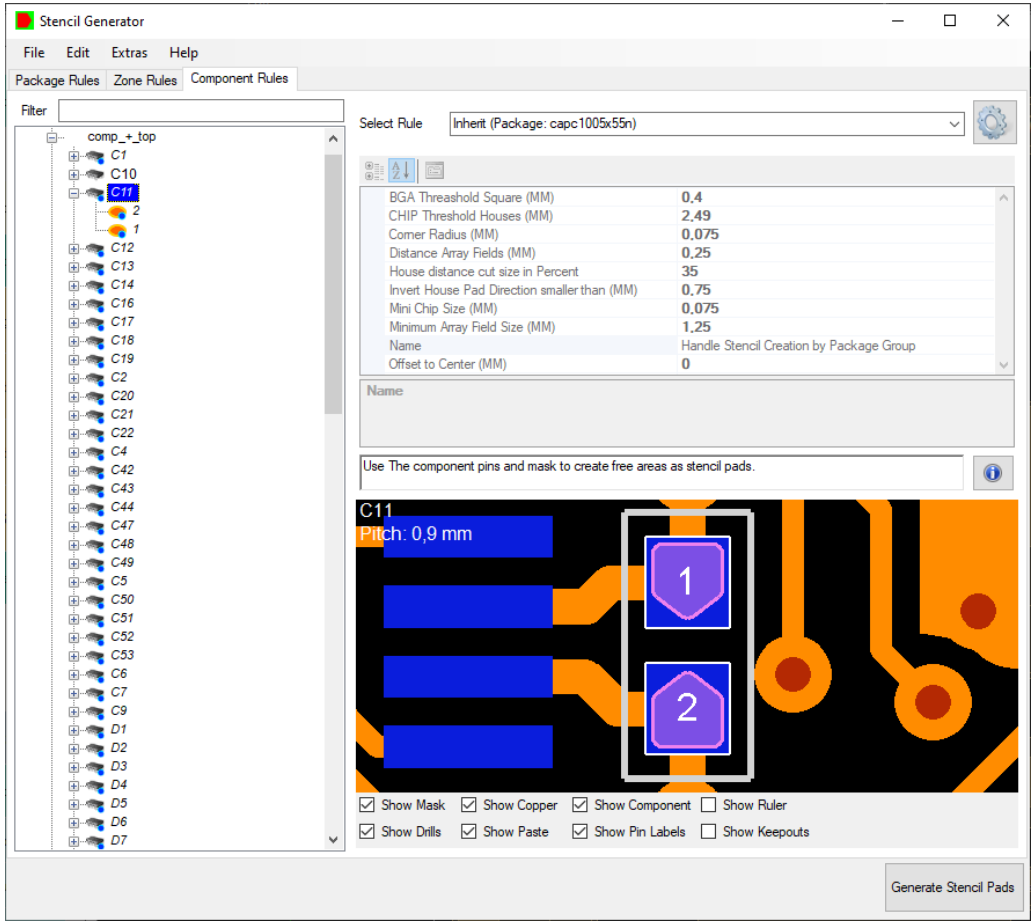


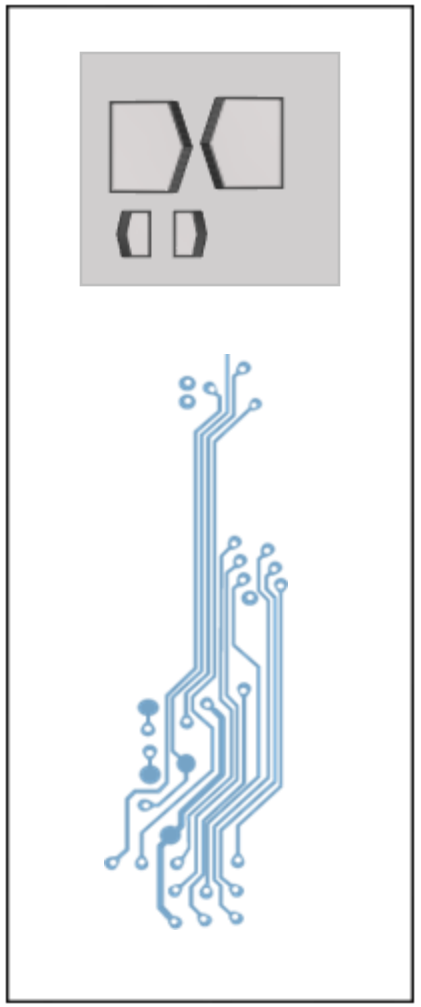
Stencil Generator



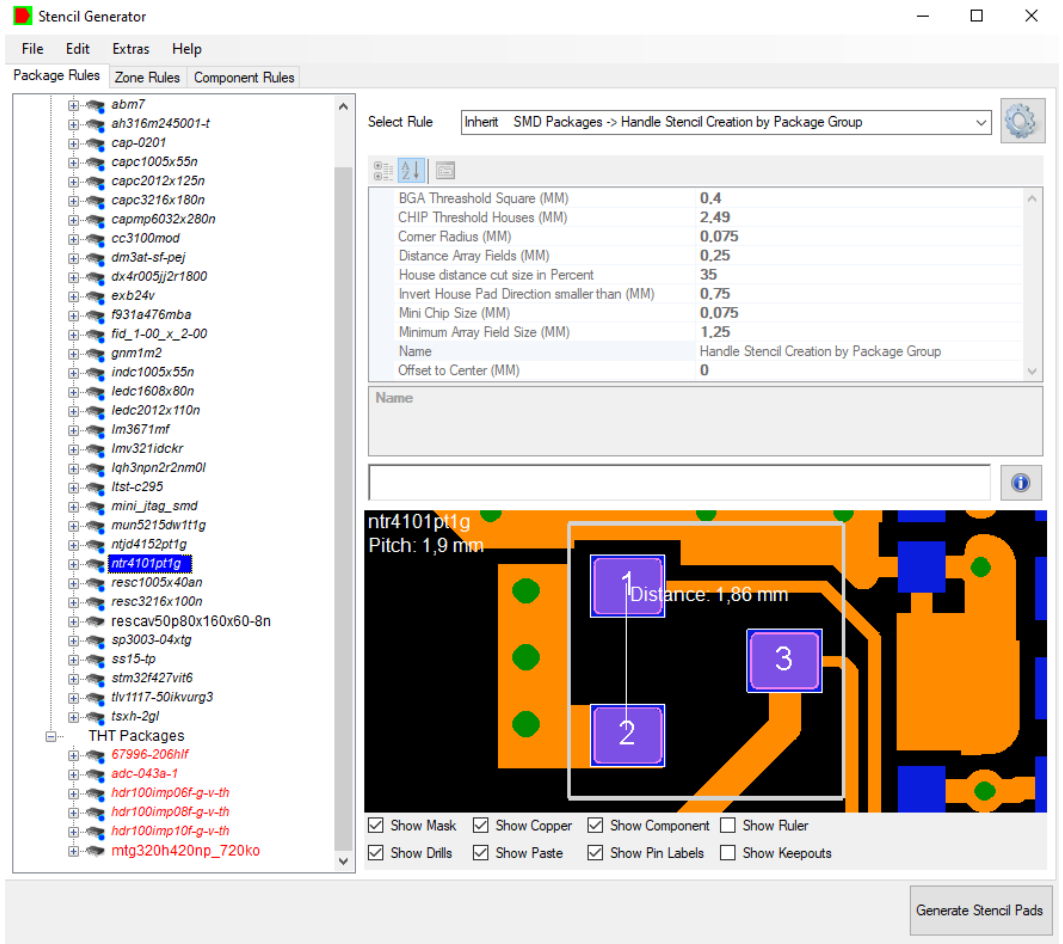
Set extra rules for components in defined zones



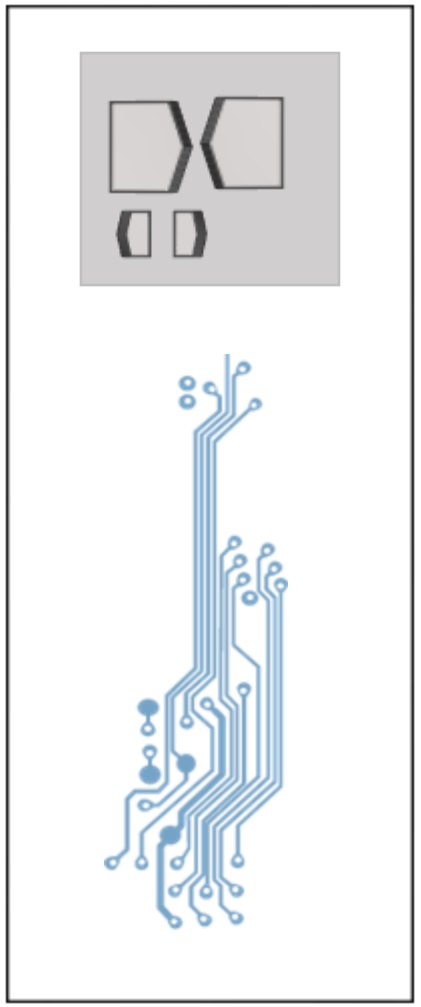
Stencil Generator



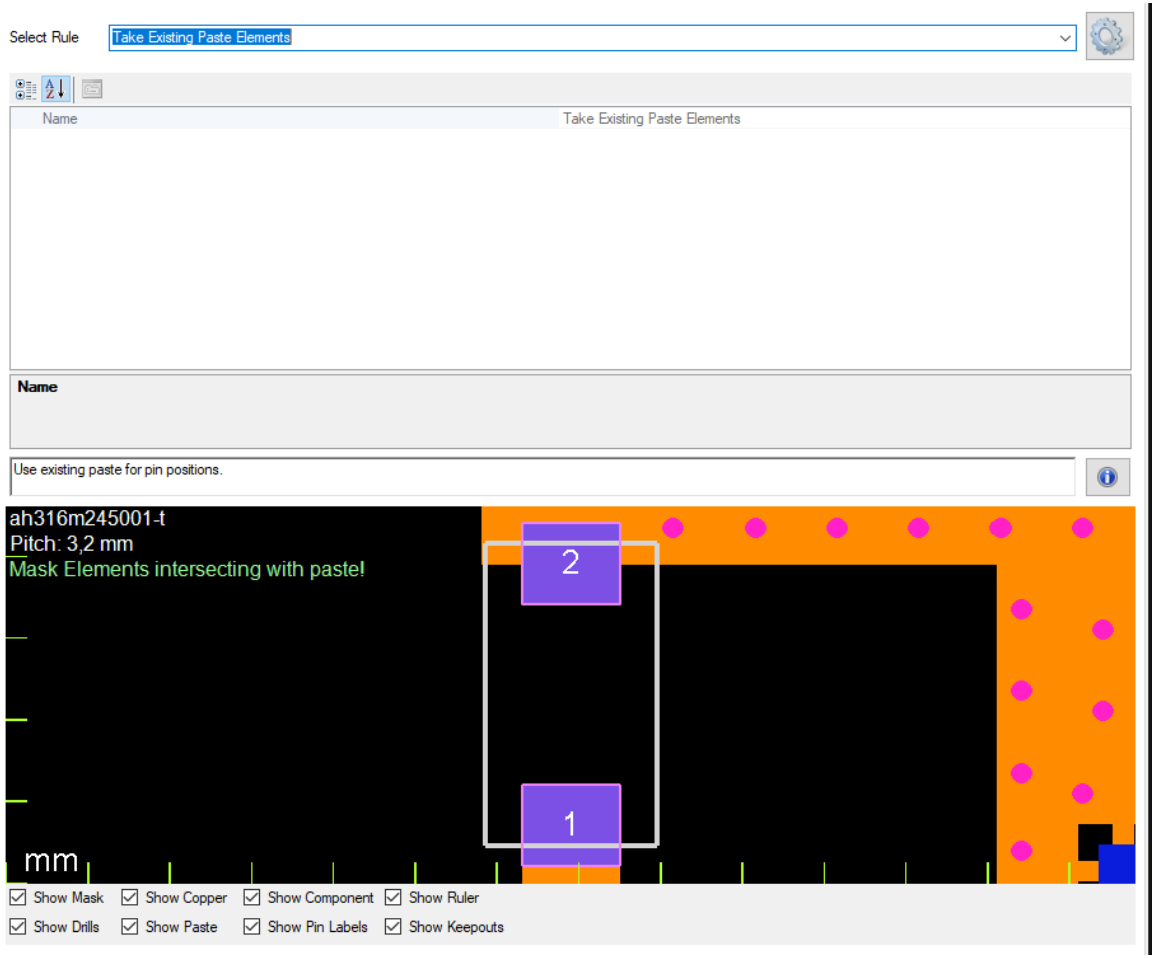
Integrated measure system in preview



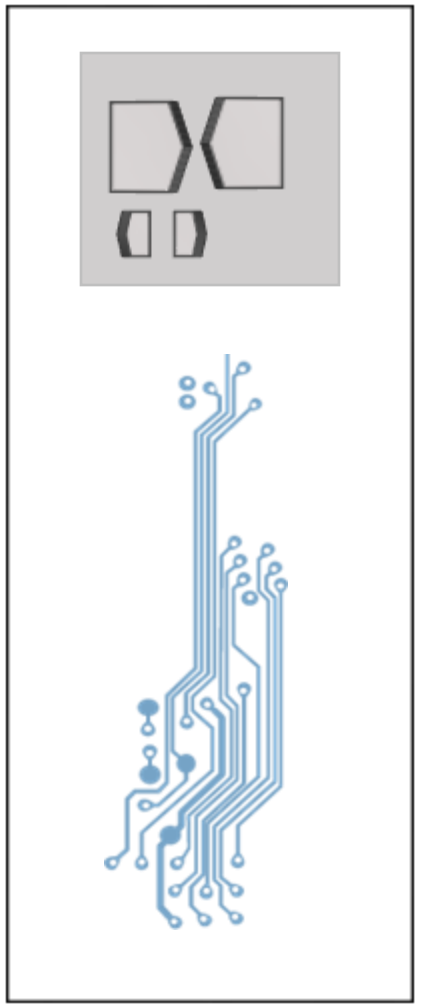
Stencil Generator



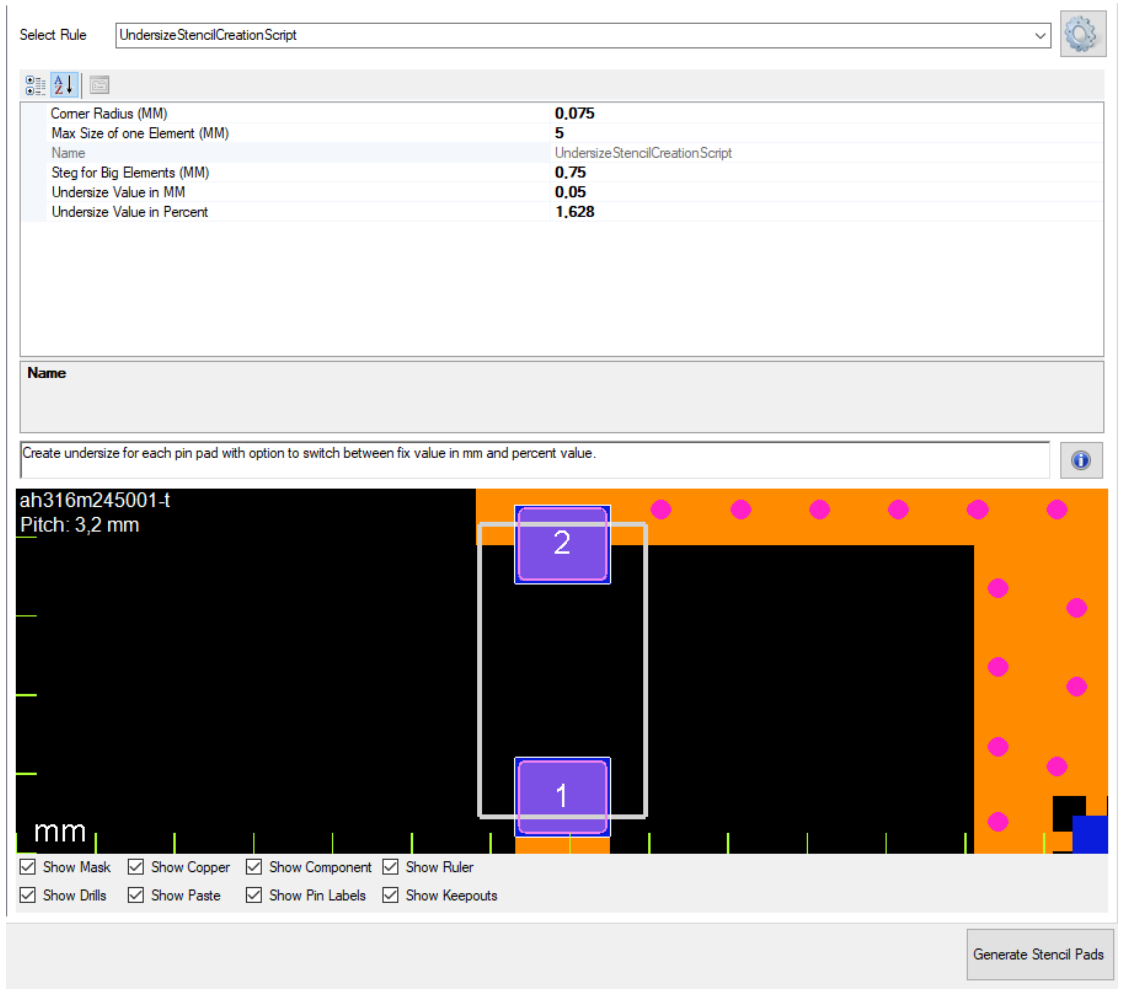
Take existing paste elements



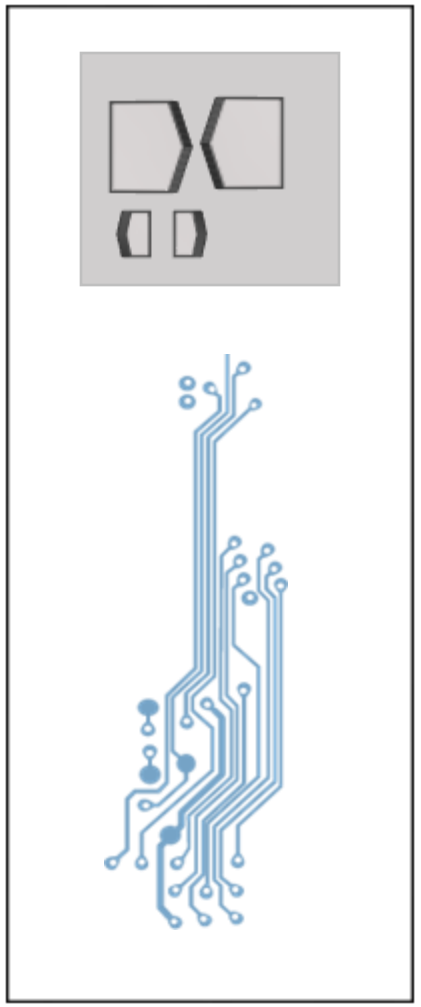
Stencil Generator



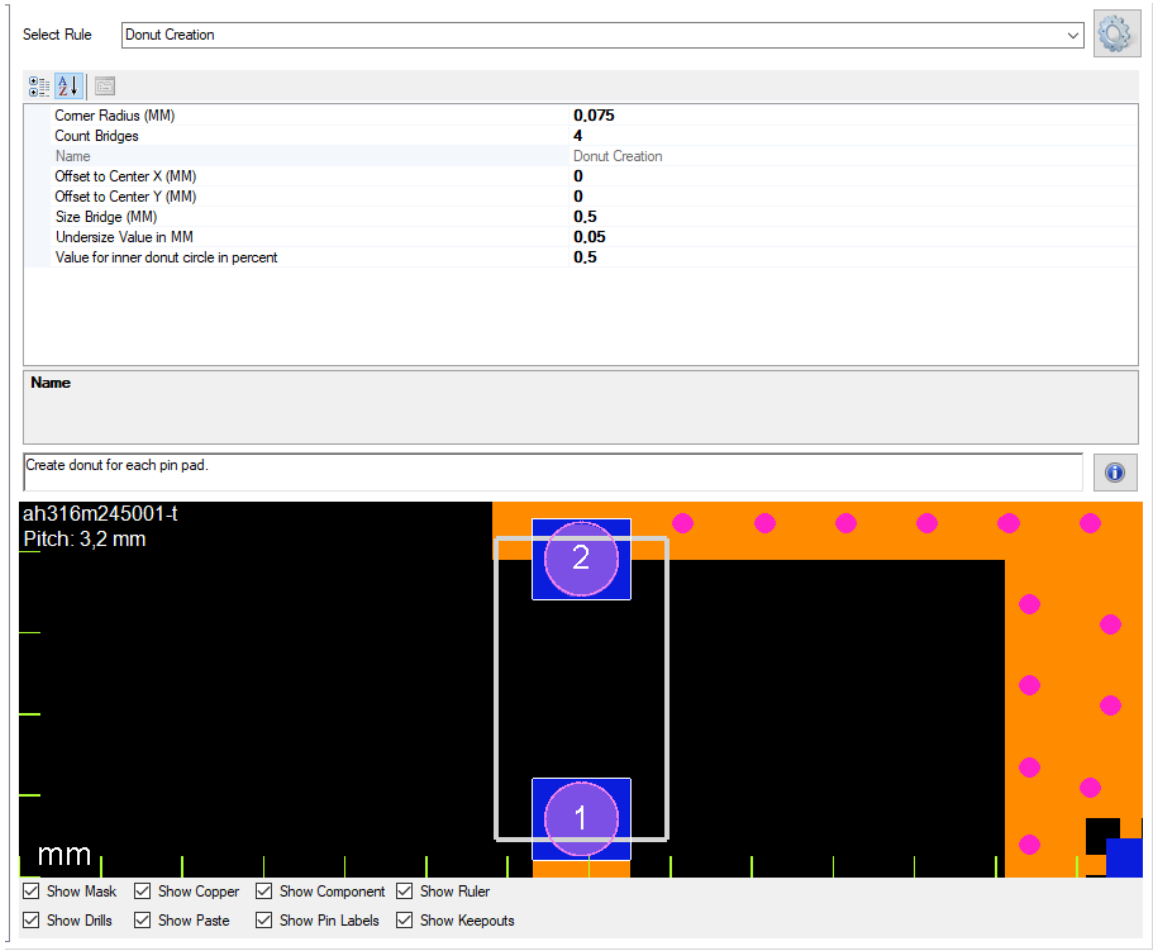
Undersize original pads



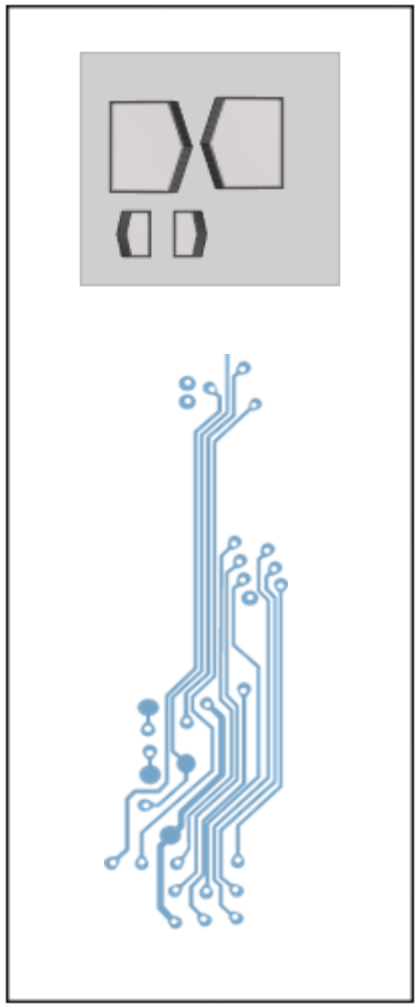
Stencil Generator



Create donat pads



Stencil Generator



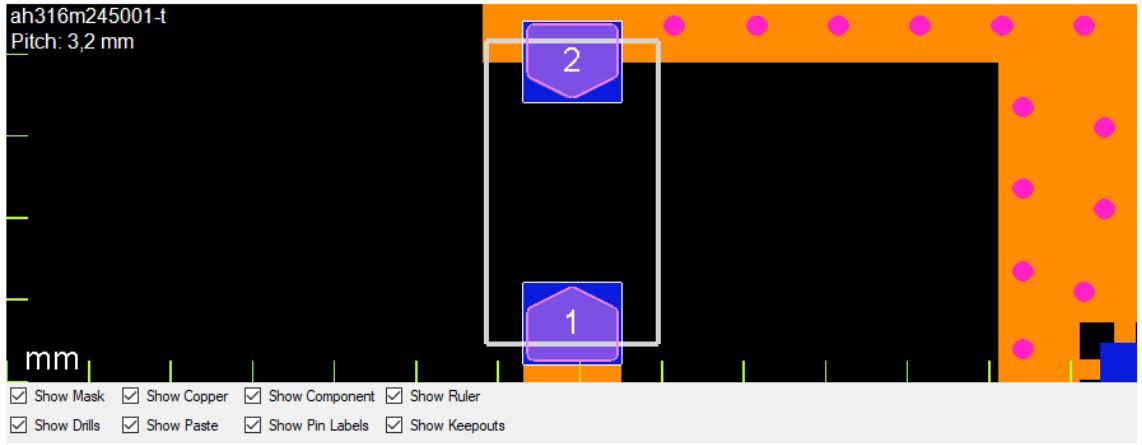
Create house pads

Select Rule: HouseBuilder

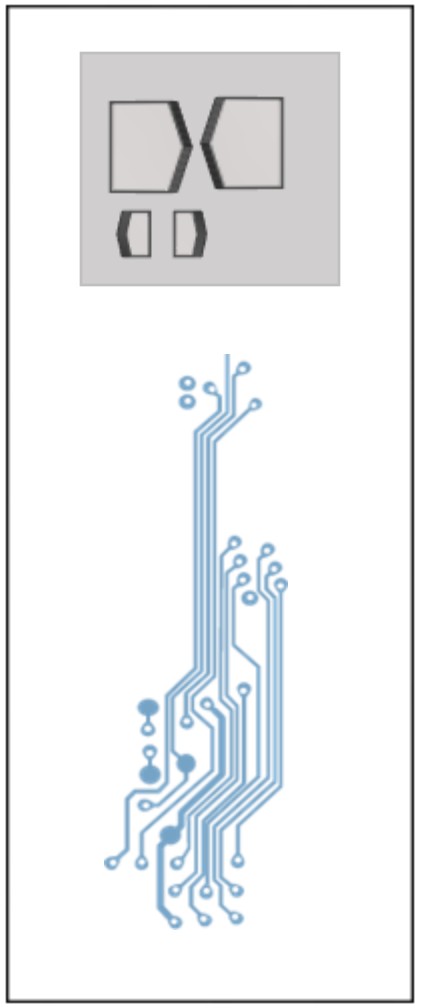
Corner Radius (MM)	0,075
House distance cut size in Percent	30
Invert Direction	False
Name	HouseBuilder
Offset to Center (MM)	0
Undersize Value (MM)	0,05

Name

Create pads in form of small houses.



Stencil Generator



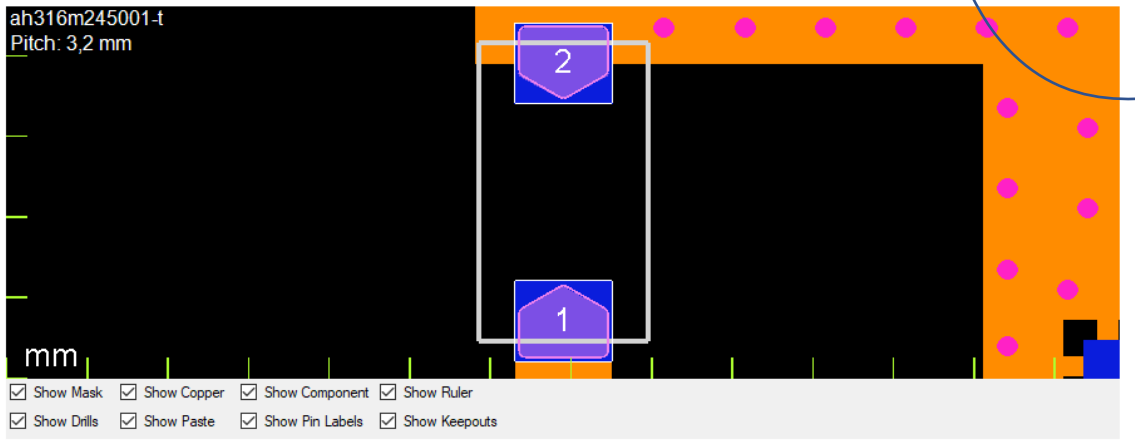
Handle pad creation by package group

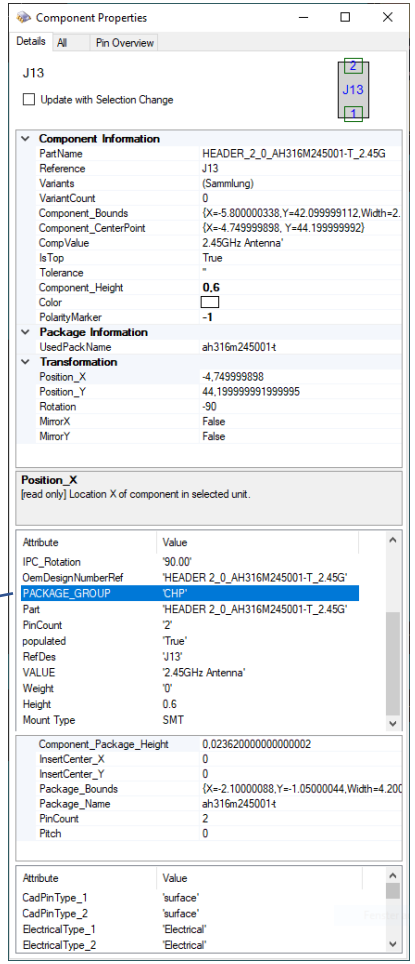
Select Rule: Handle Stencil Creation by Package Group

BGA Threashold Square (MM)	0,4
CHIP Threshold Houses (MM)	2,49
Corner Radius (MM)	0,075
Distance Array Fields (MM)	0,25
House distance cut size in Percent	35
Invert House Pad Direction smaller than (MM)	0,75
Mini Chip Size (MM)	0,075
Minimum Array Field Size (MM)	1,25
Name	Handle Stencil Creation by Package Group
Offset to Center (MM)	0
Undersize Value (MM)	0,05
Utilization Array Area (%)	40

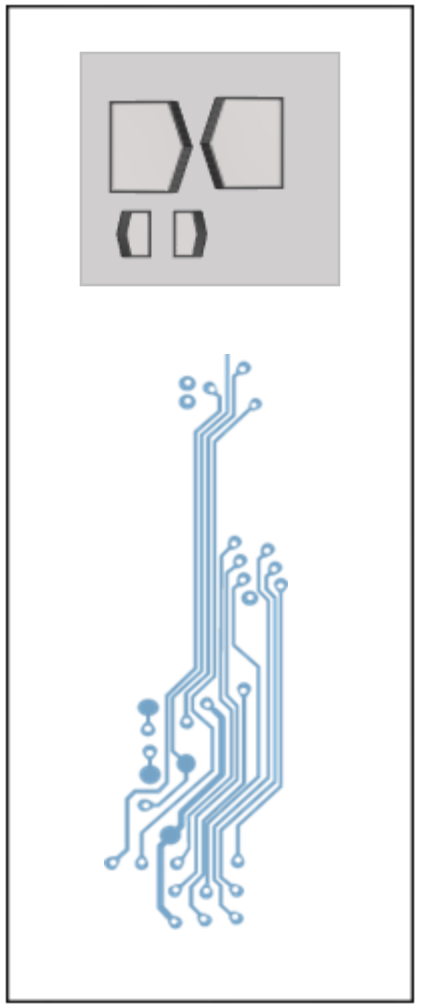
Name

Handle each stencil generation by package group property, e.g. a CHIP will handled different to SOIC and DPak.





Stencil Generator

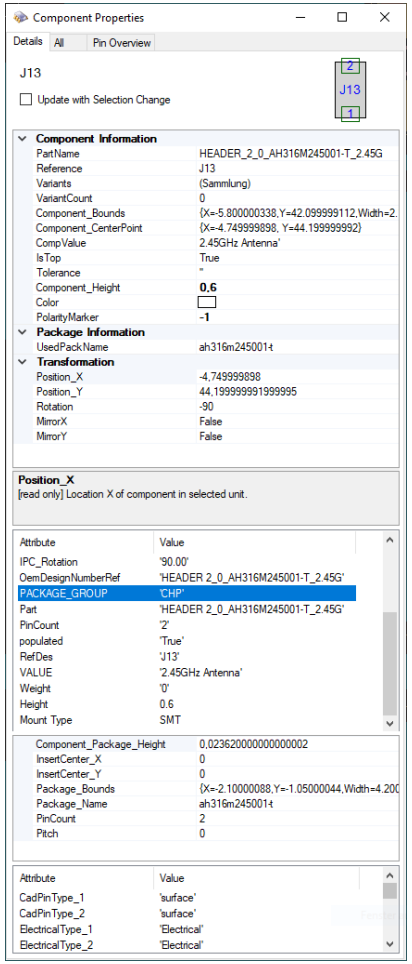


Handle pad creation by package group

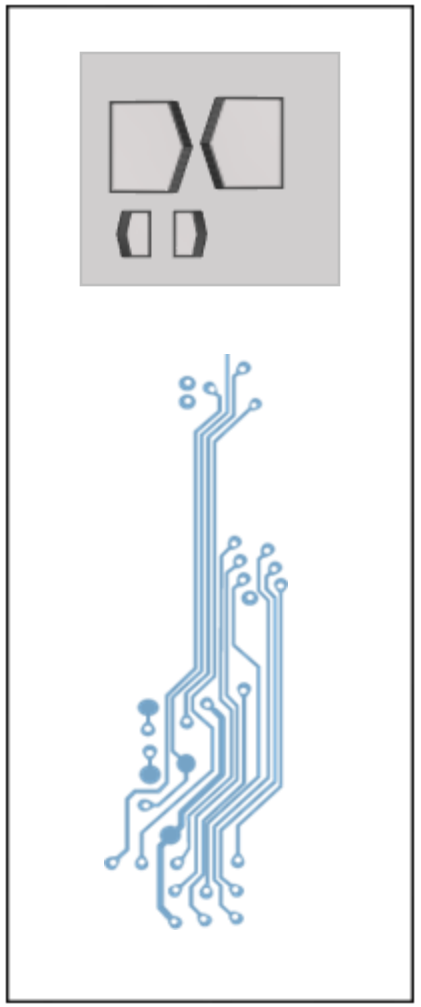
Predefined package groups

"D_MELF":
"R_MELF":
"SOP":
"QFN":
"QFP":
"DFN":
"SOT":
"SOIC":
"NETWORK":
"SOD":
"C_MOLDED":
"D_MOLDED":
"RESISTOR":
"CAPACITOR":
"TANTAL":
"DIODE":
"RESONATOR":
"INDUCTOR":
"DPAK":
"LED":
"C_ARRAY":
"R_ARRAY":

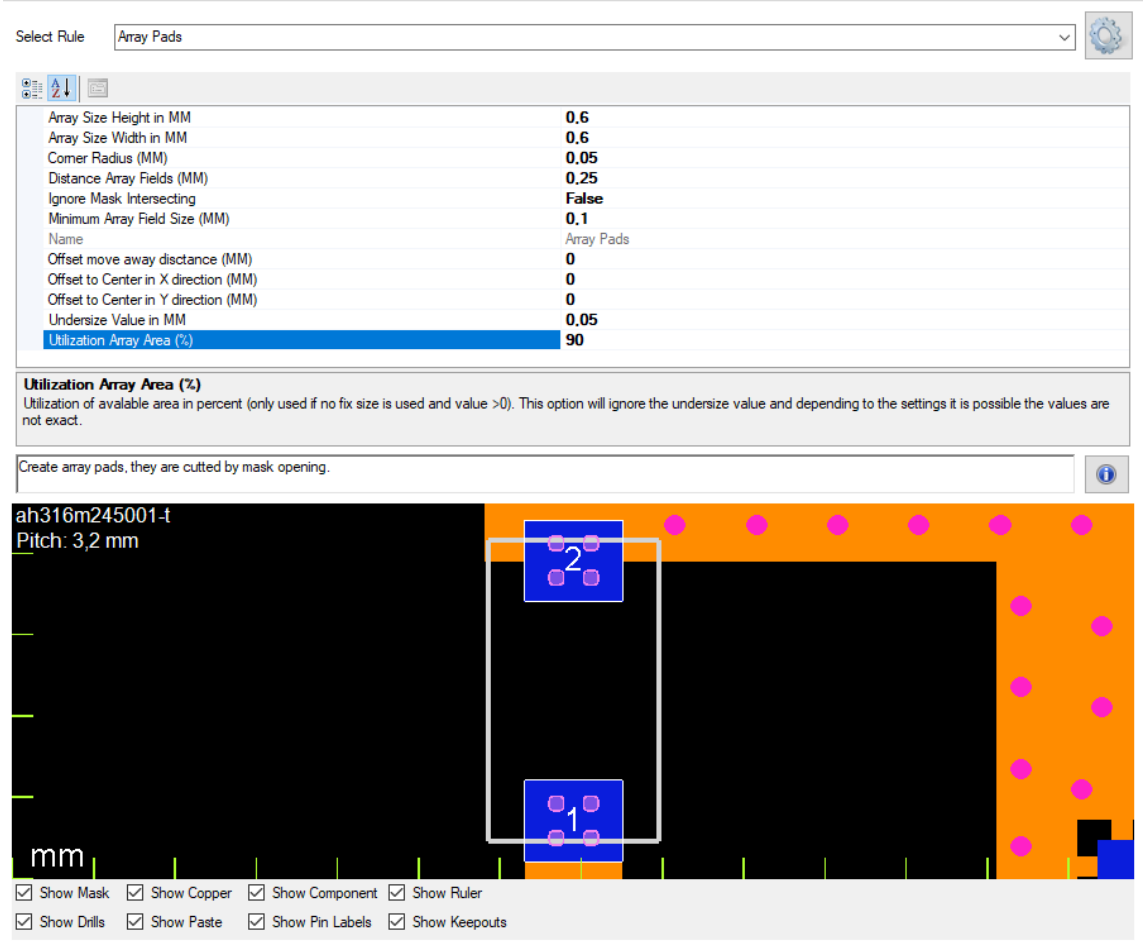
"CONNECTOR_SMT":
"CONNECTOR_THT":
"FIDUCIAL_CIRCLE":
"FIDUCIAL_RECT":
"FIDUCIAL_CROSS":
"FIDUCIAL":
"LASER":
"OTHER":
"IGNORE":
"DMC":
"BBS":
"NOT_PLACED":
"CAE":
"COIL":
"CHP":
"L_CHP":
"R_CHP":
"C_CHP":
"F_CHP":



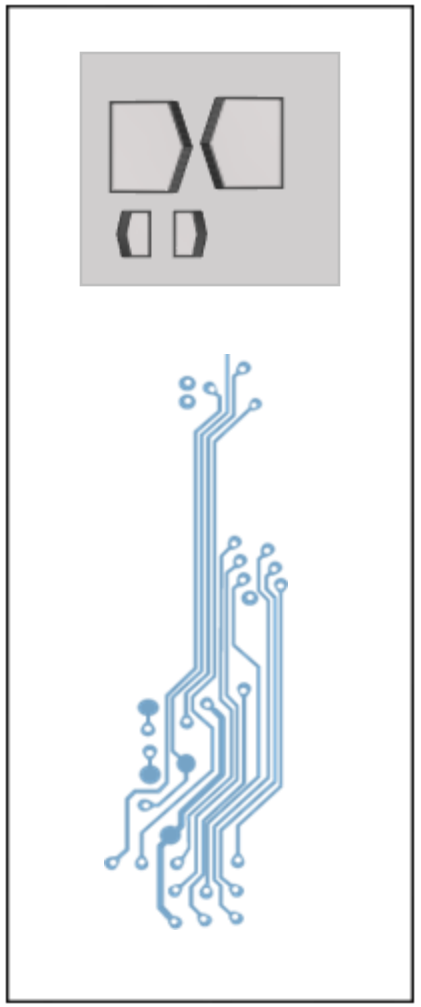
Stencil Generator



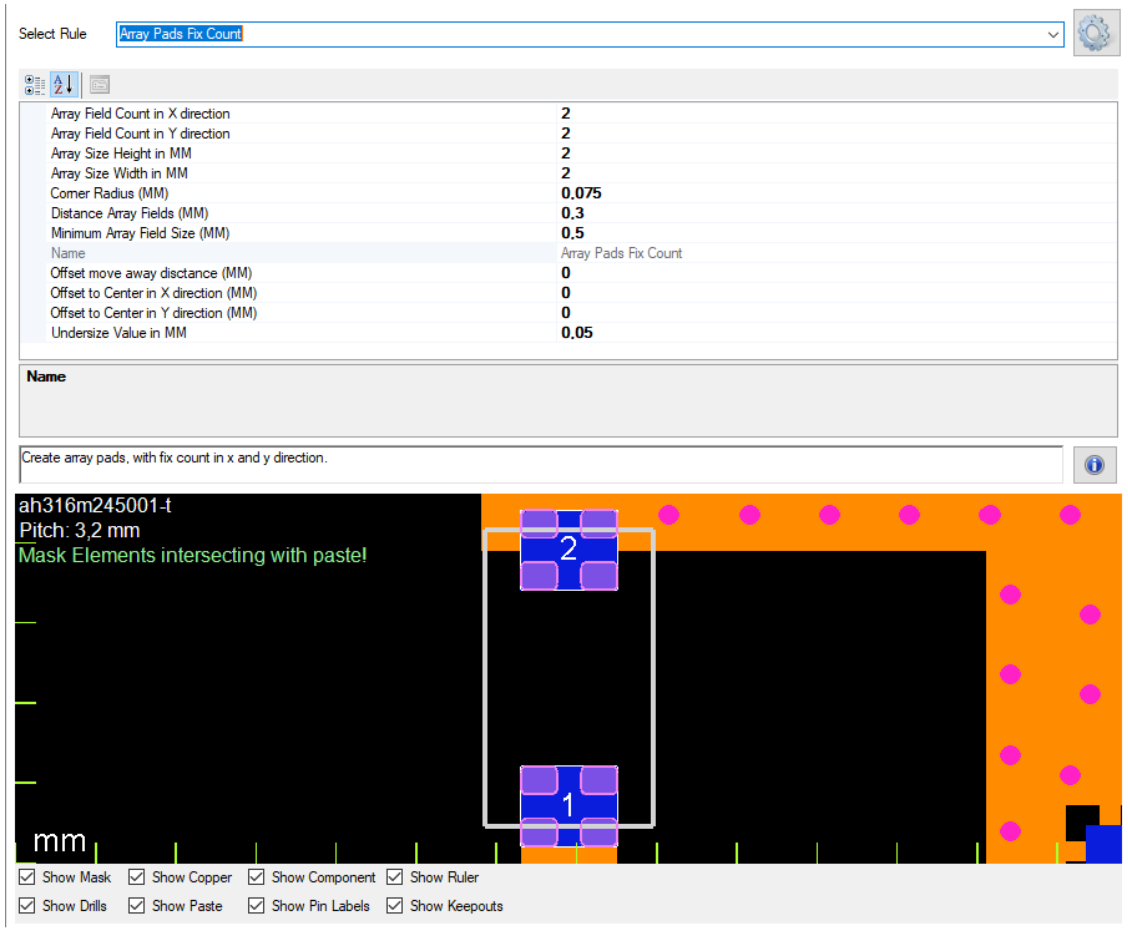
Array pads



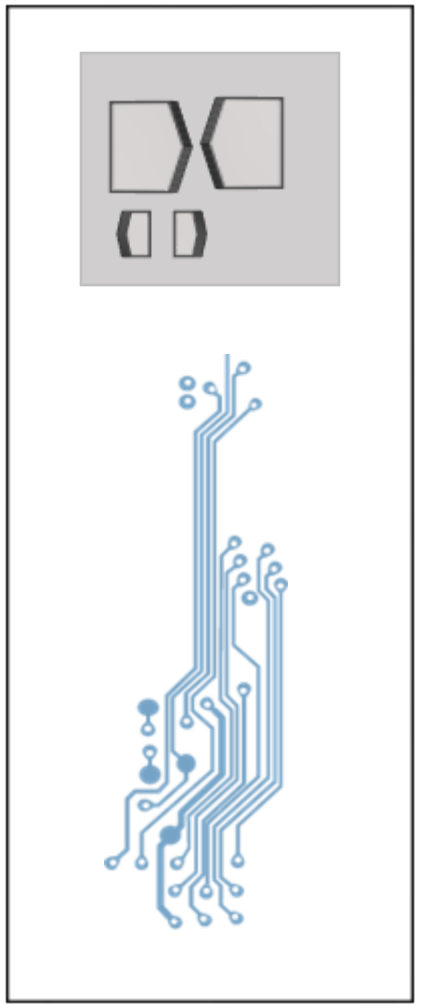
Stencil Generator



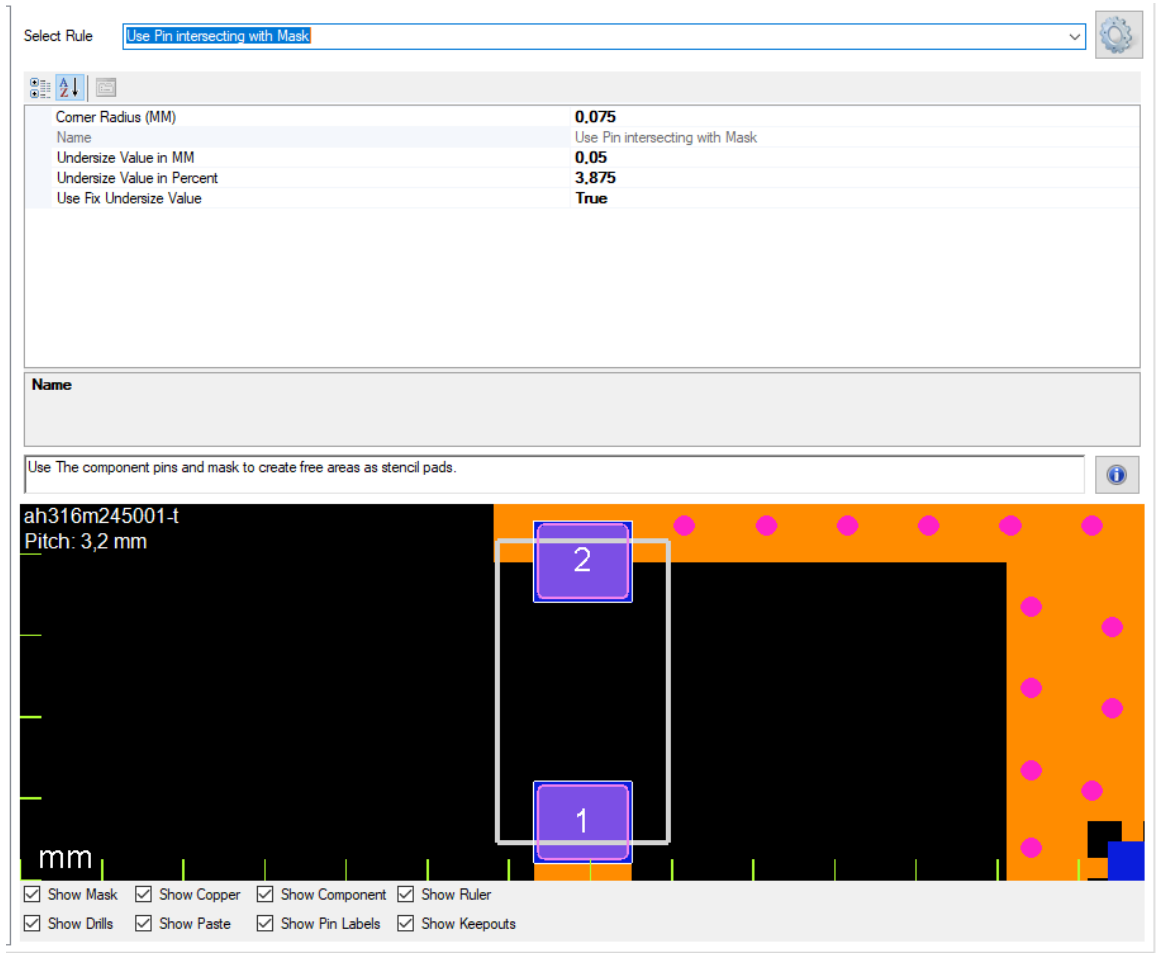
Array pads fixed count



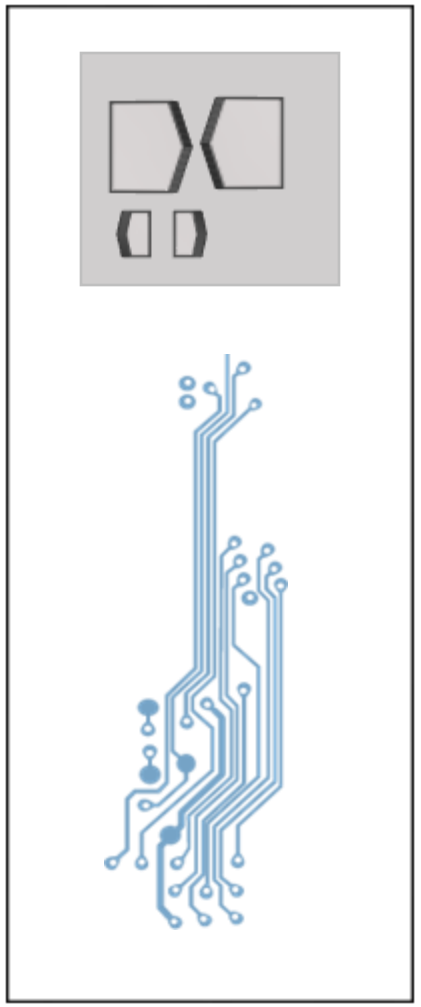
Stencil Generator



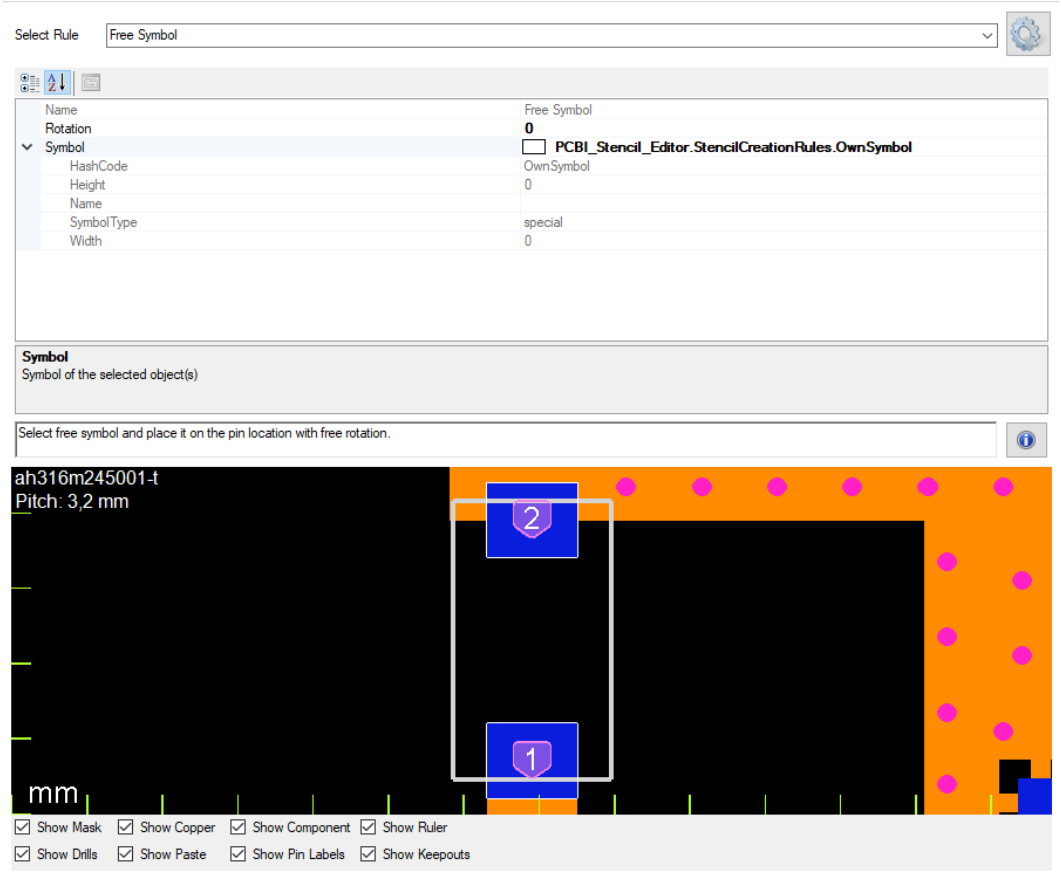
Use pin intersecting with solder mask

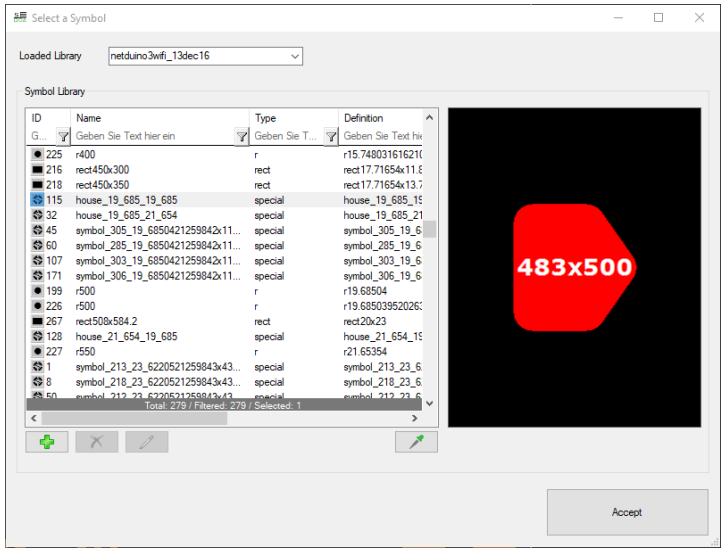


Stencil Generator



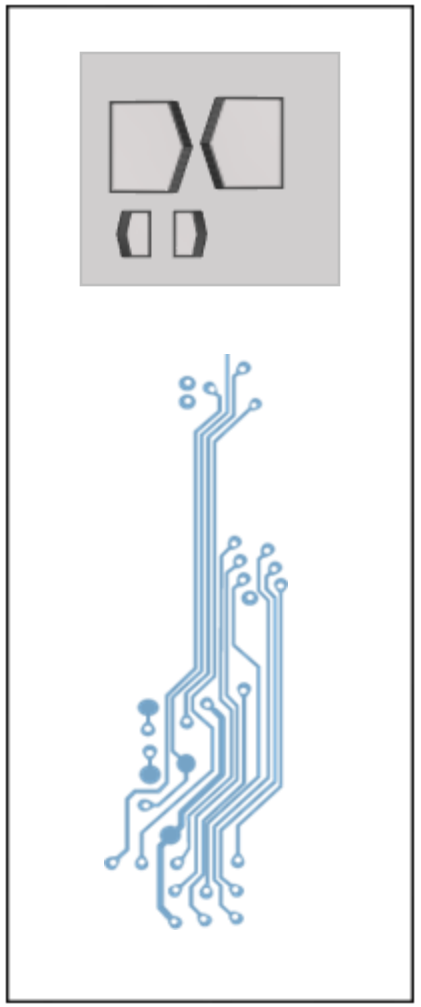
Change symbol



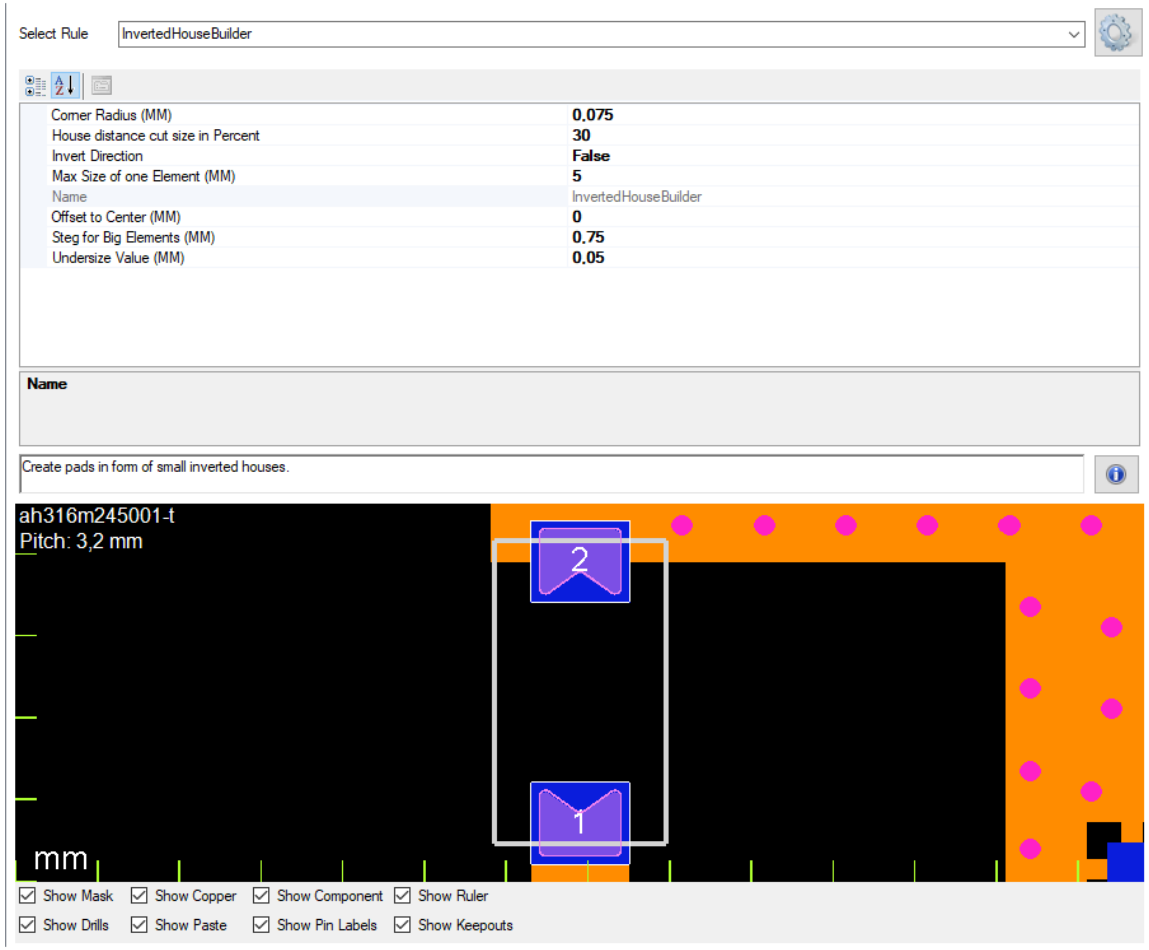


Insert symbols from job or from library

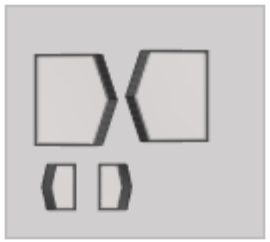
Stencil Generator



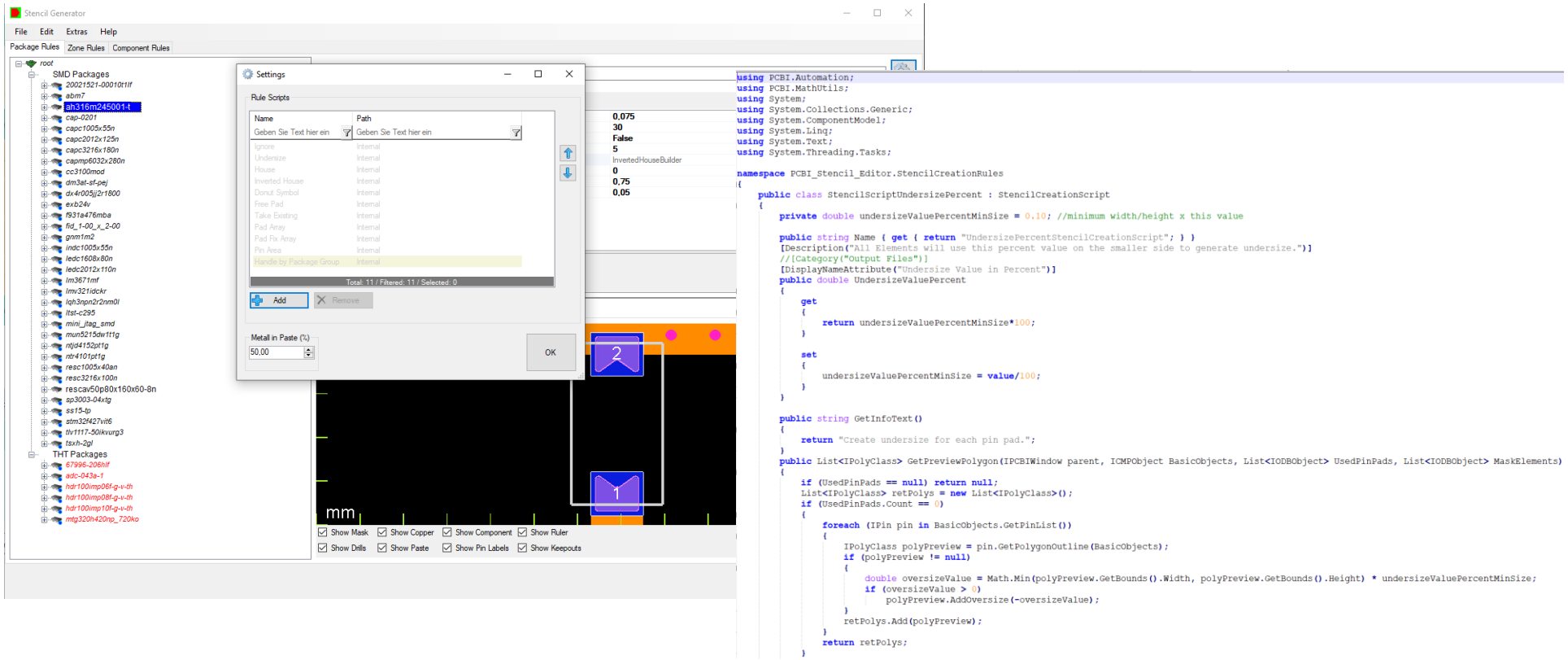
Inverted house pad



Stencil Generator



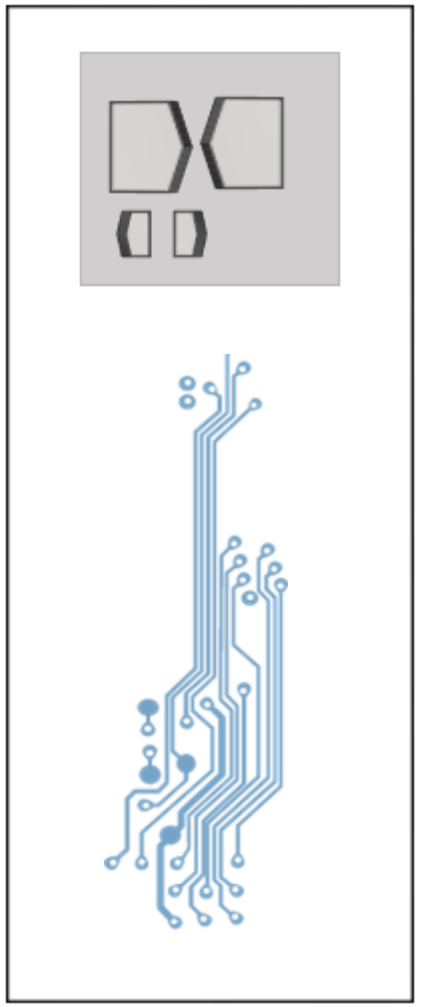
Add own rules to your stencil automation



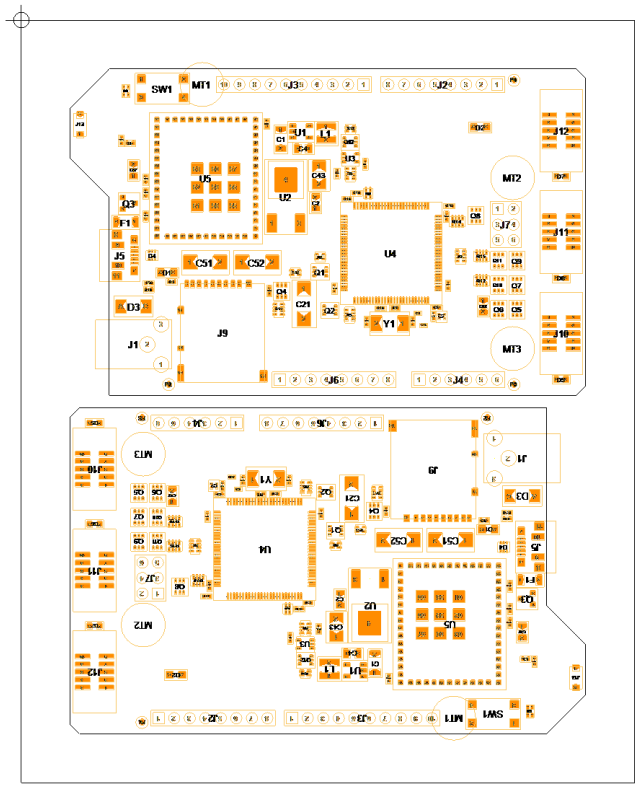

```
using PCBI.Automation;
using PCBI.MathUtils;
using System;
using System.Collections.Generic;
using System.ComponentModel;
using System.Linq;
using System.Text;
using System.Threading.Tasks;

namespace PCBI_Stencil_Editor.StencilCreationRules
{
    public class StencilScriptUndersizePercent : StencilCreationScript
    {
        private double undersizeValuePercentMinSize = 0.10; //minimum width/height x this value

        public string Name { get { return "UndersizePercentStencilCreationScript"; } }
        [Description("All Elements will use this percent value on the smaller side to generate undersize.")]
        //[Category("Output Files")]
        [DisplayNameAttribute("Undersize Value in Percent")]
        public double UndersizeValuePercent
        {
            get
            {
                return undersizeValuePercentMinSize*100;
            }

            set
            {
                undersizeValuePercentMinSize = value/100;
            }
        }

        public string GetInfoText()
        {
            return "Create undersize for each pin pad.";
        }
        public List<IPolyClass> GetPreviewPolygon(IPCBIWindow parent, ICMPObject BasicObjects, List<IODBObject> UsedPinPads, List<IODBObject> MaskElements)
        {
            if (UsedPinPads == null) return null;
            List<IPolyClass> retPolys = new List<IPolyClass>();
            if (UsedPinPads.Count == 0)
            {
                foreach (IPin pin in BasicObjects.GetPinList())
                {
                    IPolyClass polyPreview = pin.GetPolygonOutline(BasicObjects);
                    if (polyPreview != null)
                    {
                        double oversizeValue = Math.Min(polyPreview.GetBounds().Width, polyPreview.GetBounds().Height) * undersizeValuePercentMinSize;
                        if (oversizeValue > 0)
                            polyPreview.AddOversize(-oversizeValue);
                    }
                    retPolys.Add(polyPreview);
                }
                return retPolys;
            }
```

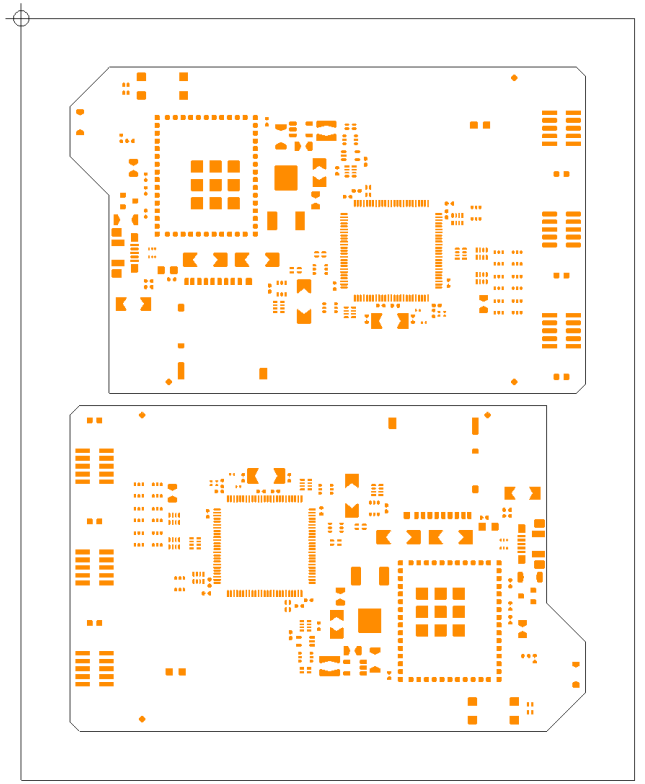
Interface: StencilCreationScript

Panel

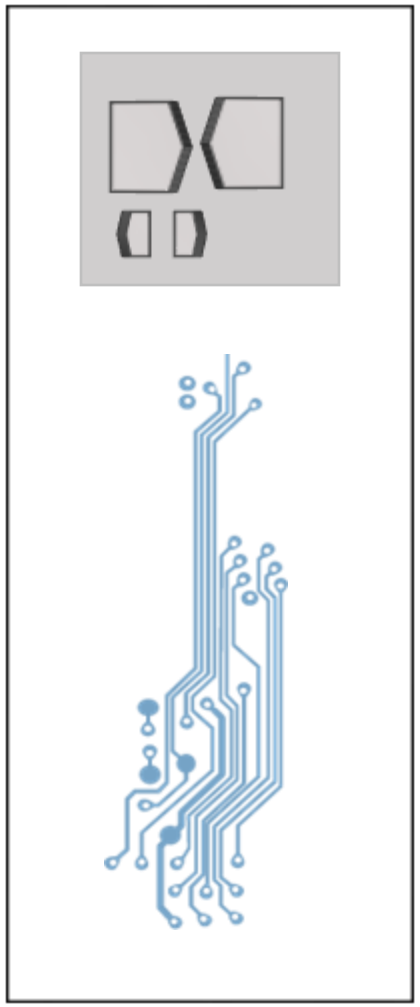


Send the stencil data in your preferred format to your supplier

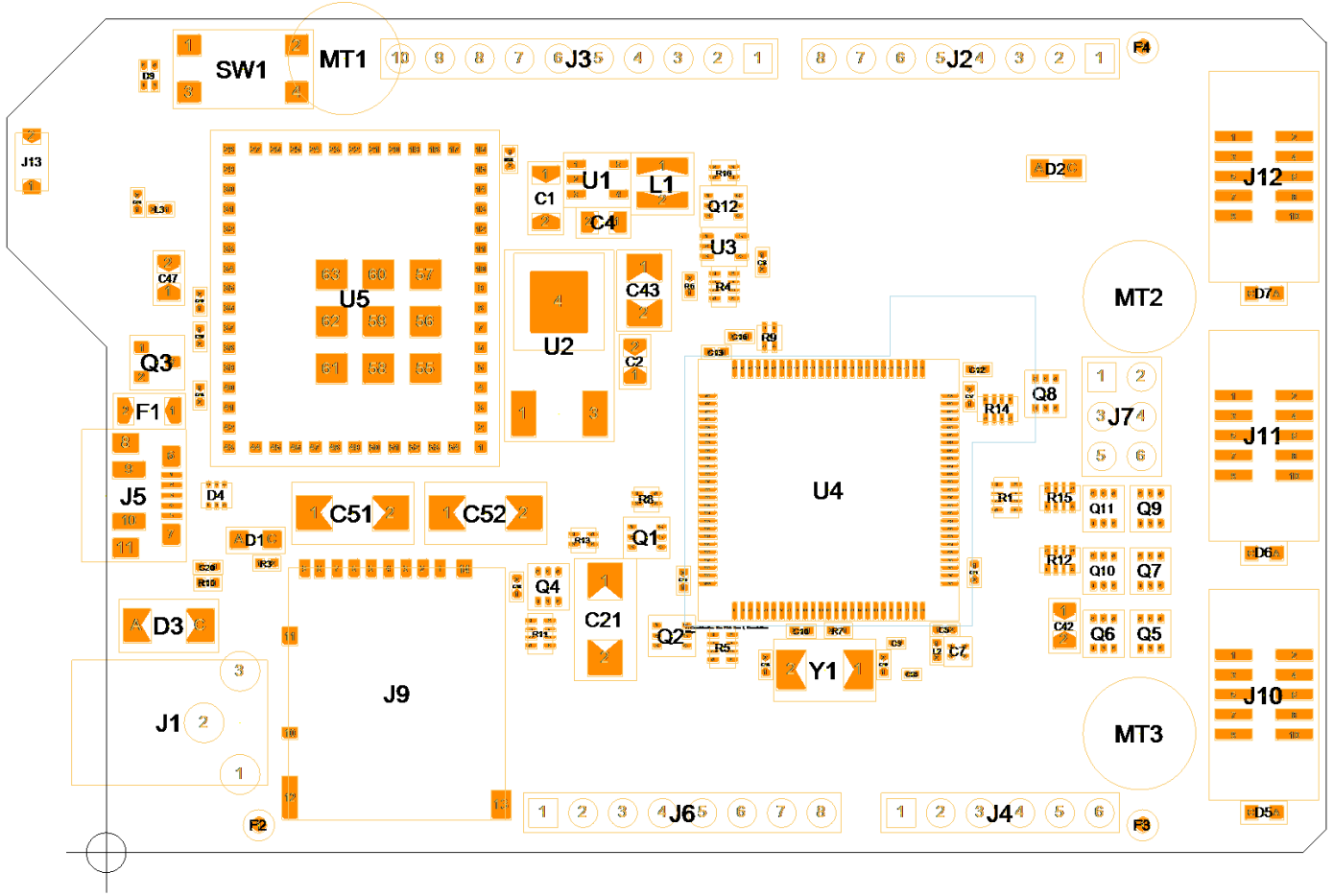




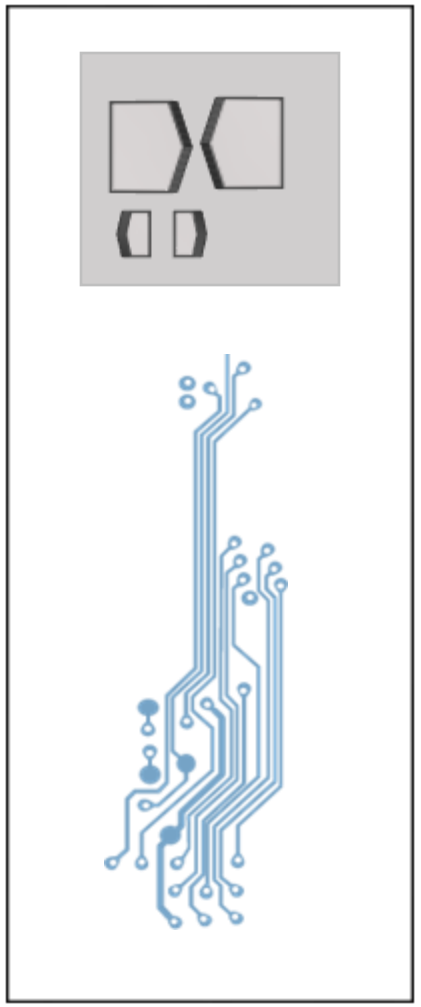
Stencil Generator



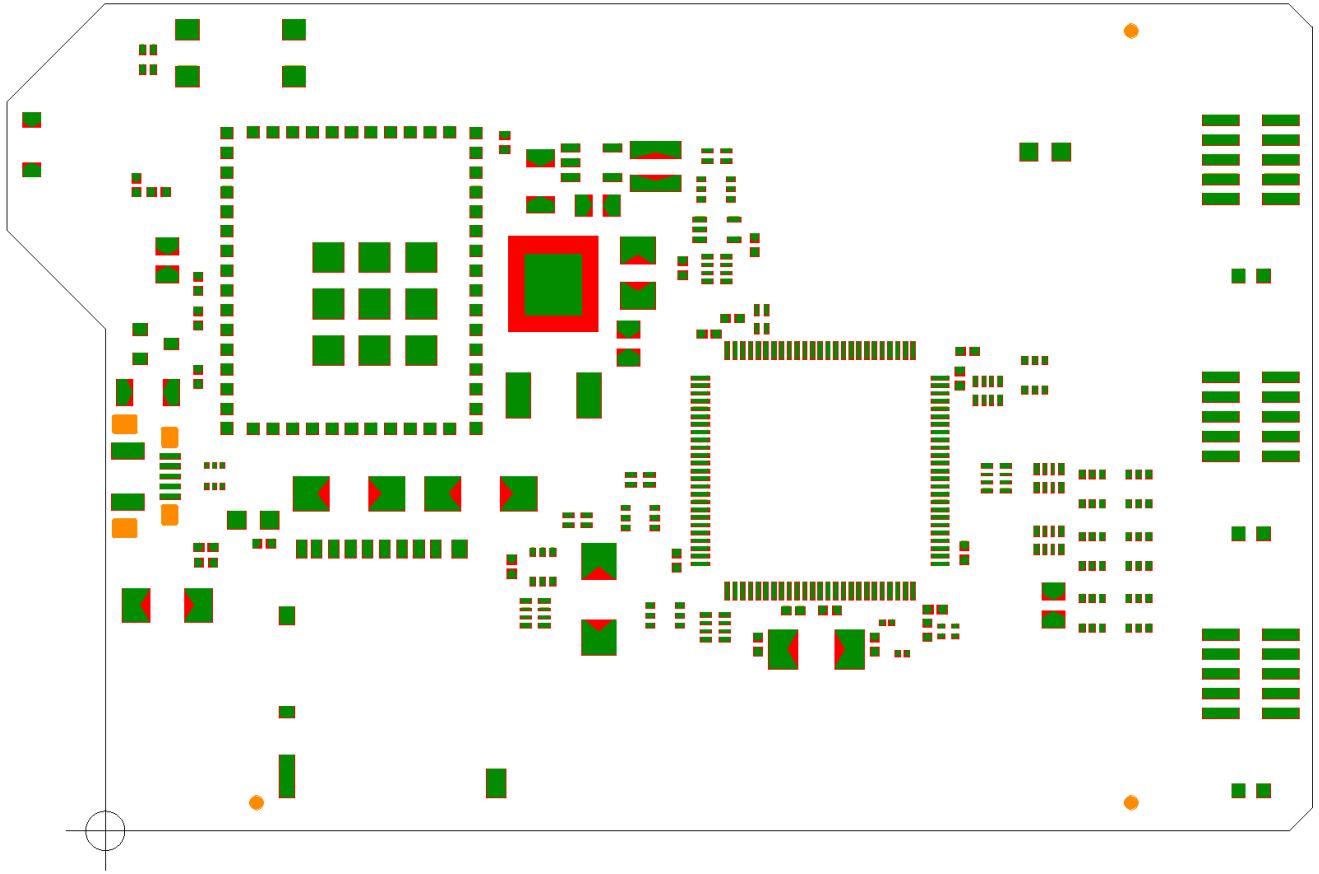
Result of the rule-based stencil wizard



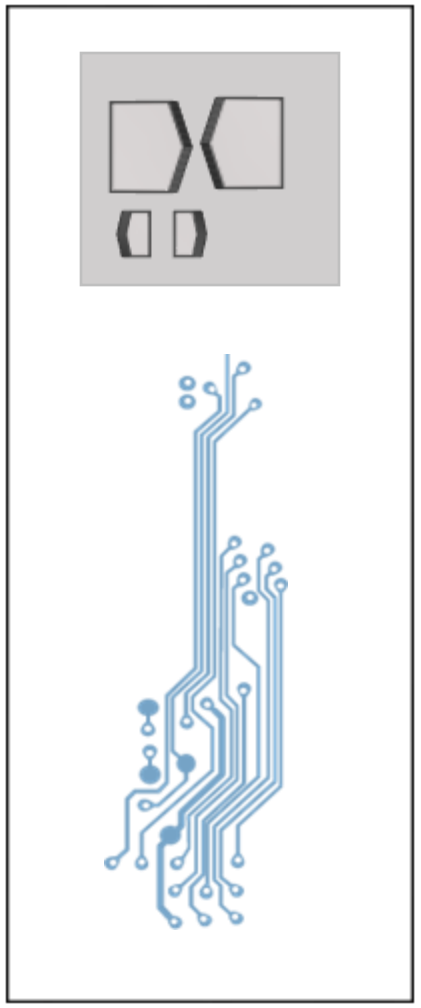
Stencil Generator



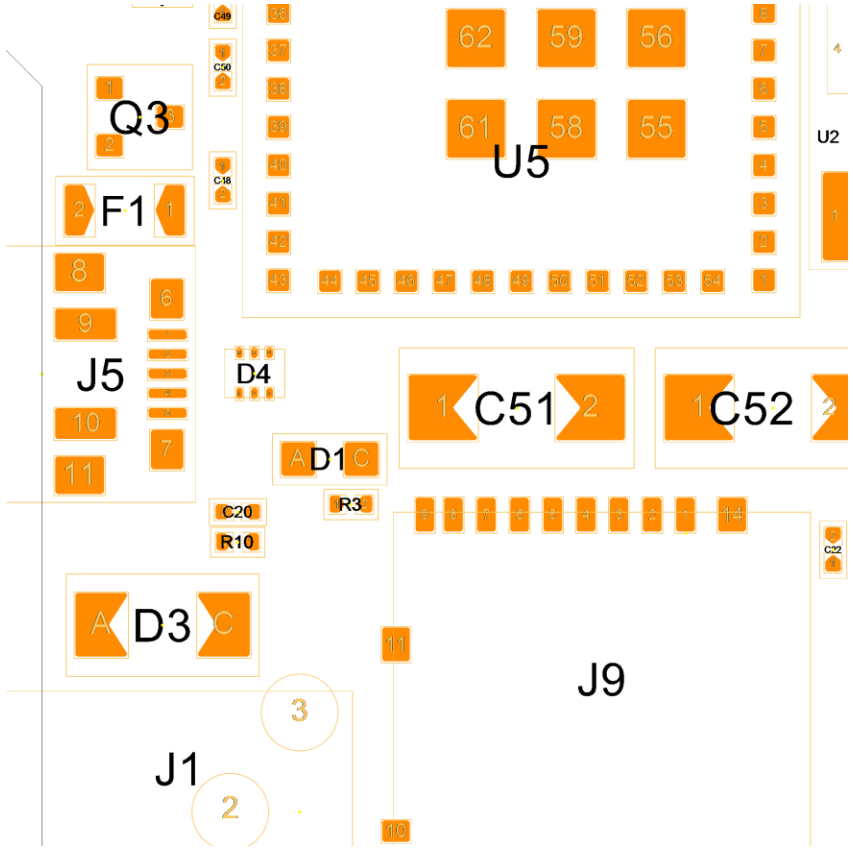
Before and after



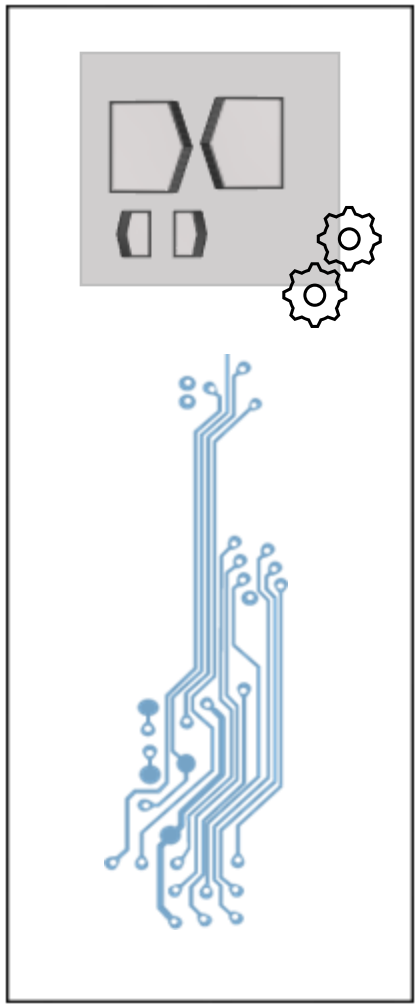
Stencil Generator



Stencil pad details



Stencil Analyzer



Get Paste Size Ratio

File Edit Help

Ratio Help

IPC-7525 May 2000

Table 1 General Aperture Design Guidelines for Surface-Mount Devices

Part Type	Pitch	Pad Footprint Width	Pad Footprint Length	Aperture Width	Aperture Length	Stencil Foil Thickness Range	Aspect² Ratio Range	Area Ratio Range
PLCC	1.25 mm [49.2 mil]	0.65 mm [25.6 mil]	2.00 mm [78.7 mil]	0.60 mm [23.6 mil]	1.95 mm [76.8 mil]	0.15 - 0.25 mm [5.91 - 9.84 mil]	2.3 - 3.8	0.88 - 1.48
QFP	0.65 mm [25.6 mil]	0.35 mm [13.8 mil]	1.50 mm [59.1 mil]	0.30 mm [11.8 mil]	1.45 mm [57.1 mil]	0.15 - 0.175 mm [5.91 - 6.89 mil]	1.7 - 2.0	0.71- 0.83
QFP	0.50 mm [19.7 mil]	0.30 mm [11.8 mil]	1.25 mm [49.2 mil]	0.25 mm [9.84 mil]	[1.20 mm] 47.2 mil	0.125 - 0.15 mm [4.92 - 5.91 mil]	1.7 - 2.0	0.69 - 0.83

Stencil thickness: 120 µm

Mark lines with ratio < 0.66

Use individual Thickness for existing zones

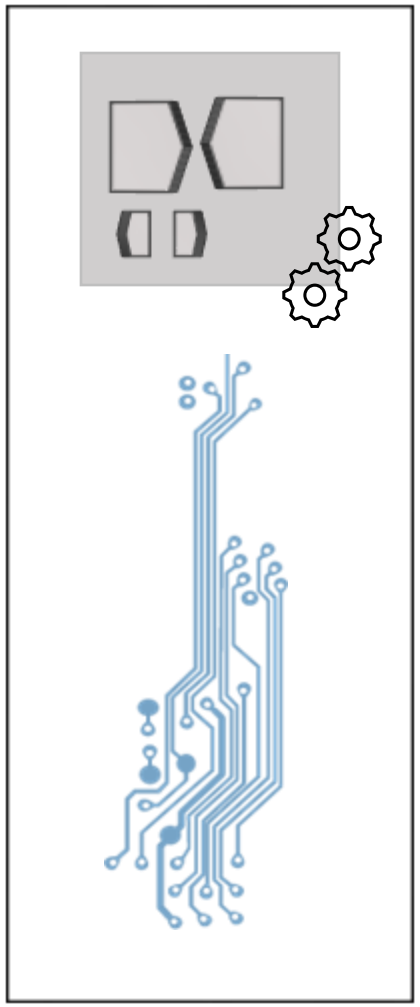
Check only in PCB Profile

Calculate

CSV Export

Close

Stencil Ratios



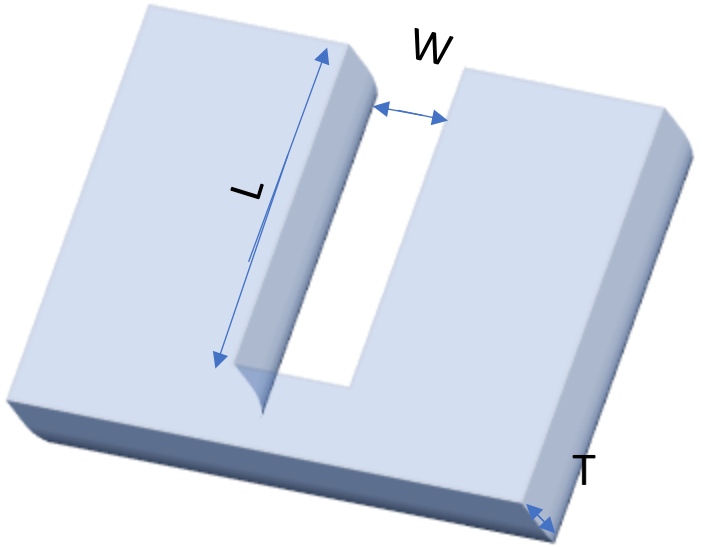
Solder Paste Stencil Ratios
In order to ensure efficient transfer of solder paste from a stencil aperture to a pad during the soldering process, there are two main ratios to consider:

•**Aspect ratio**: the relation between the width of narrowest aperture and the thickness of the stencil. This ratio should be at least 1.5.

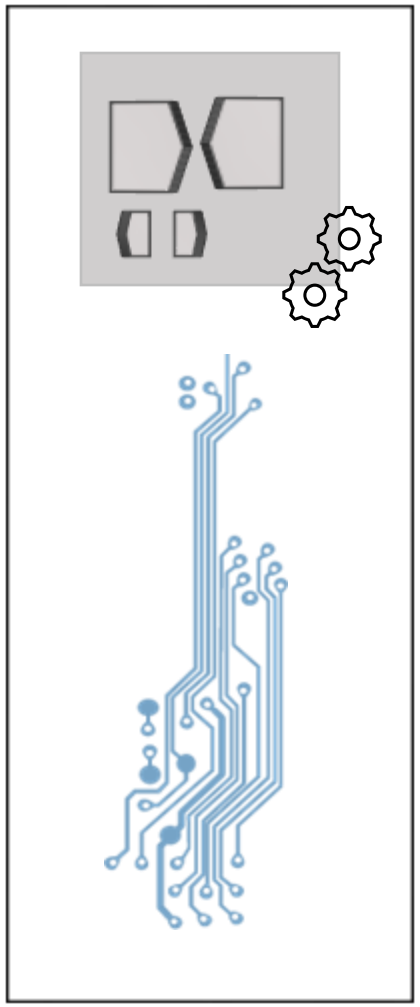
•**Area ratio**: gives a more accurate and detailed indication of a stencil's paste release performance. This is the ratio between the area of the aperture and the area of the hole walls. This ratio should be at least 0.66.

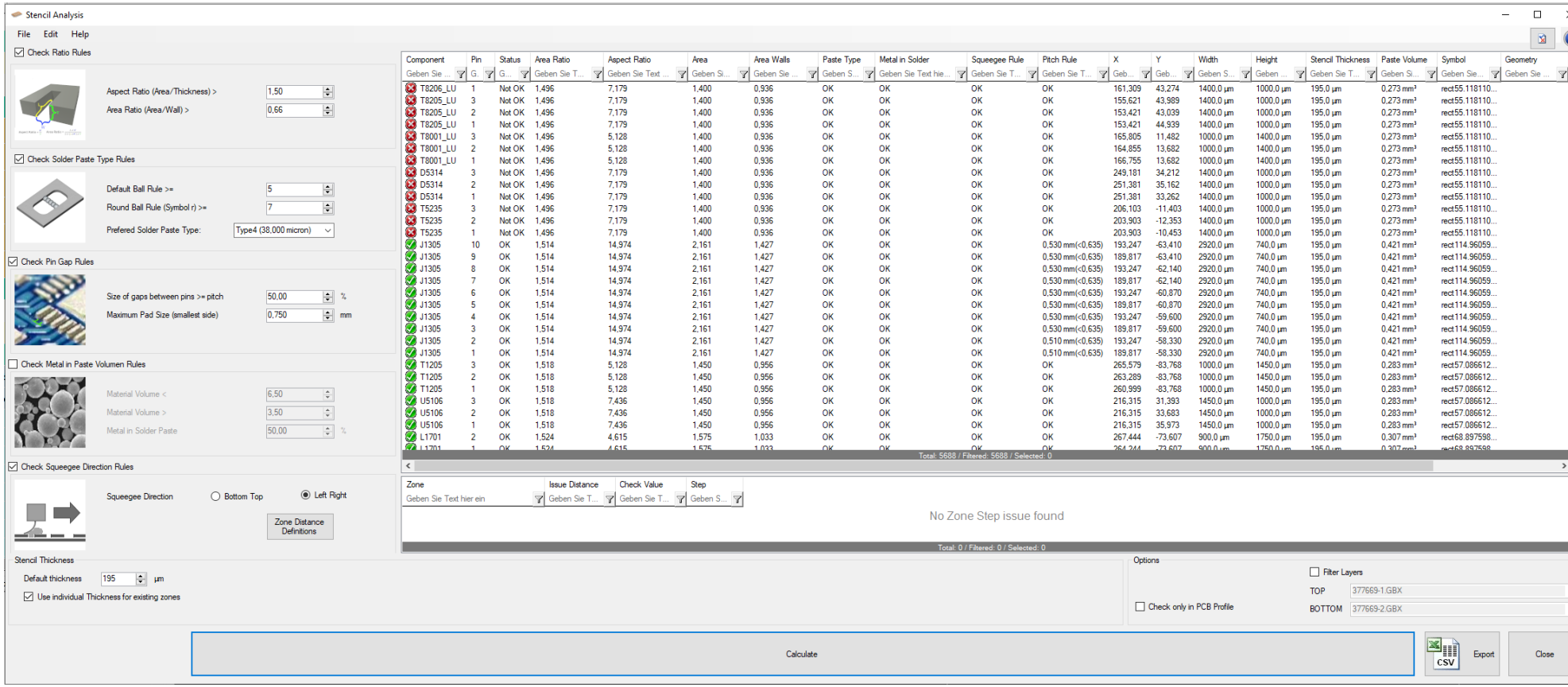
Aspect Ratio = W / T

Area Ratio = A (Pad) / A (Wall)

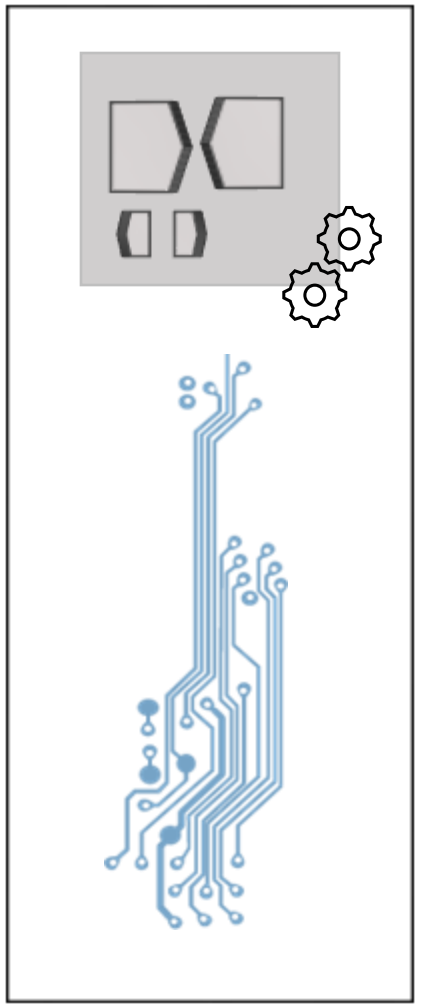


Stencil analyzer

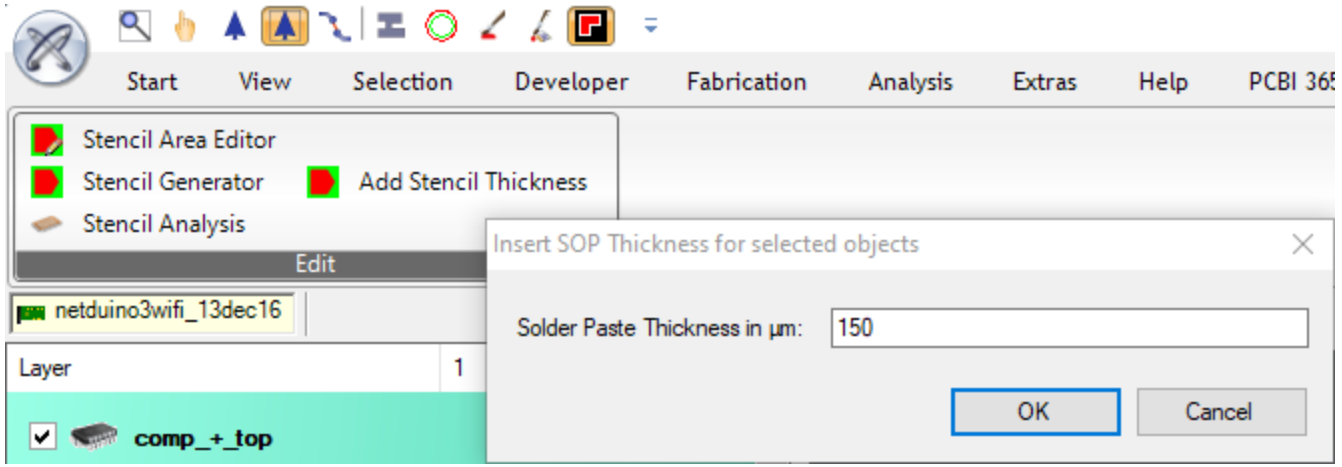




Stencil Wizard



Global stencil thickness



You can set the thickness in the ODB++ attribute, the value is used in the SPI exports e.g. by Viscom to set different values for the paste thickness.
Note: If you do not save the zone values in the ODB attribute, they will not be recognized during export.

Request Customized Functions

Get in touch,
info@easylogix.de
Guenther Schindler
Tel. +49 941 568 136 26

Useful Links:

PCB-Investigator
www.pcb-investigator.com

PCBi-Physics
www.PCBi-Physics.com

Native Board Import (3D Interface to CATIA, SiemensNX, SolidWorks, SolidEdge)
www.sts-development.biz

GerberLogix
www.gerberLogix.com

Online Gerber Viewer
www.Gerber-Viewer.com

Software Development, CAD Converter, data connection
www.easyLogix.de

In conclusion, PCB-Investigator is a powerful and versatile tool that can streamline the PCB design and manufacturing process. It offers a wide range of features and capabilities that can help to improve efficiency, reduce costs, and ensure the highest quality of your final product. Whether you are a designer, manufacturer, or engineer, PCB-Investigator is an essential tool for any professional working in the PCB industry. With its ability to automate and streamline various processes, it can help you to achieve your goals and stay ahead of the competition.