EASYLOGIX.DE

PCB-Investigator

Creepage Analysis / Hazard Analysis

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Why Creepage Analysis is important

Creepage analysis is the study of the electrical path that a current follows on a printed circuit board (PCB) or other electrical component. It is important for several reasons:

- Safety: Creepage analysis helps to identify areas where electrical current may be able to jump across an insulating material, potentially causing a short circuit or electrical shock. By identifying these areas, engineers can design PCBs that are safer to use.

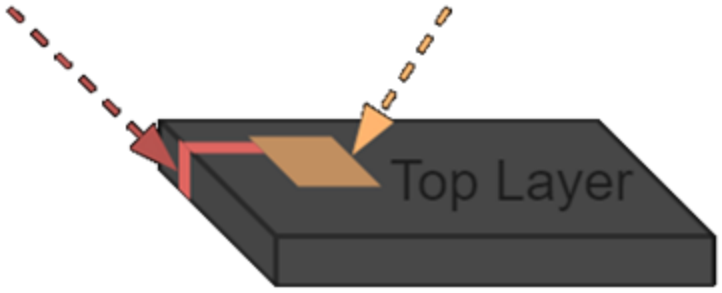
- Reliability: Creepage analysis helps to identify areas on a PCB where the electrical current may be able to break down the insulation, leading to component failure. By identifying these areas and designing accordingly, engineers can improve the reliability of the PCB.

- Compliance: Many electrical and electronic products are required to meet certain safety and reliability standards. Creepage analysis is often used to ensure that these standards are met.
- In summary, creepage analysis is important because it helps to ensure the safety, reliability, and compliance of electrical and electronic products.

Why Creepage Analysis is important

The **Creepage Analysis** in PCB-Investigator calculates the shortest distance from the outer edges to the conductive components to one another and to the outer egde of the board. This also considers uncoated drill holes (e.g. mount drill holes) and indentations, which otherwise would be too time consuming to calculate manually.

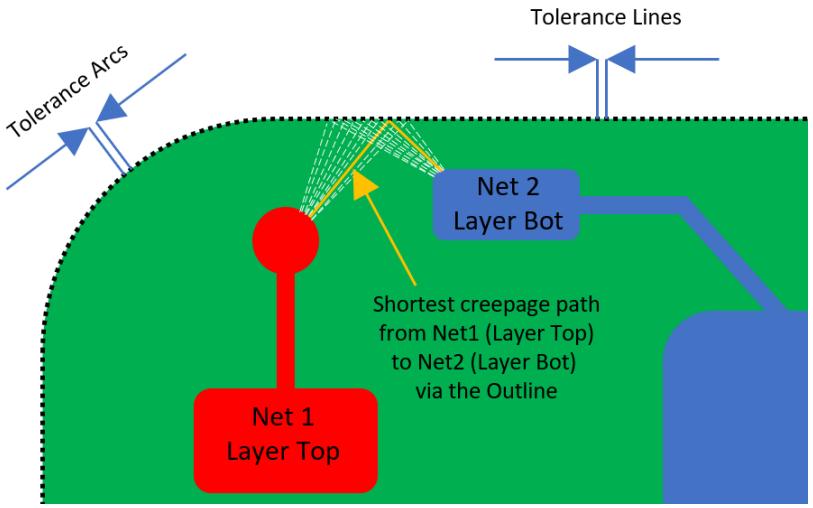
1.Net to Net creepage analysis is used to detect creepage issues between two single nets.
2.Net Group to Net Group creepage analysis has to be used to detect issues between any net of the first group to any net of thesecond group (*Note: You have to create Net Groups first. To create Net Groups use the button of the following image. Creating net groups can be found in "Net Groups", shown below)*
3.There is also an option to detect issues between a single net, or any net of a group to the board outline of the PCB

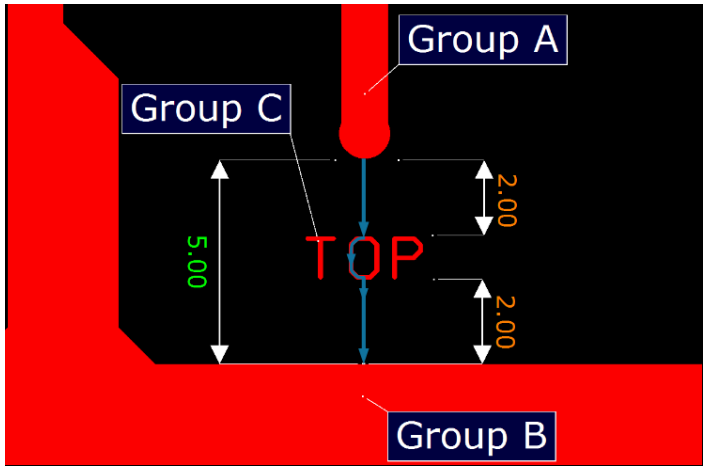


F.4 DIN EN 60664-1 (VDE 0110-1), table F.4 (extract)
Creepage distance for the avoidance of the failure by tracking

Voltage r.m.s. [1]	Minimum creepage distances								
	Printed wiring material								
	Pollution degree								
	1	2	1	2			3		
	All material groups	All material groups except IIIb	All material groups	Material group I	Material group II	Material group III	Material group I	Material group II	Material group III [2]
V	mm	mm	mm	mm	mm	mm	mm	mm	mm
25	0,025	0,040	0,125	0,500	0,500	0,500	1,250	1,250	1,250
32	0,025	0,040	0,14	0,53	0,53	0,53	1,30	1,30	1,30
40	0,025	0,040	0,16	0,56	0,80	1,10	1,40	1,60	1,80
50	0,025	0,040	0,18	0,60	0,85	1,20	1,50	1,70	1,90
63	0,040	0,063	0,20	0,63	0,90	1,25	1,60	1,80	2,00
80	0,063	0,100	0,22	0,67	0,95	1,30	1,70	1,90	2,10
100	0,100	0,160	0,25	0,71	1,00	1,40	1,80	2,00	2,20
125	0,160	0,250	0,28	0,75	1,05	1,50	1,90	2,10	2,40
160	0,250	0,400	0,32	0,80	1,10	1,60	2,00	2,20	2,50
200	0,400	0,630	0,42	1,00	1,40	2,00	2,50	2,80	3,20
250	0,560	1,000	0,56	1,25	1,80	2,50	3,20	3,60	4,00
320	0,75	1,60	0,75	1,60	2,20	3,20	4,00	4,50	5,00
400	1,0	2,0	1,0	2,0	2,8	4,0	5,0	5,6	6,3
500	1,3	2,5	1,3	2,5	3,6	5,0	6,3	7,1	8,0
630	1,8	3,2	1,8	3,2	4,5	6,3	8,0	9,0	10,0
800	2,4	4,0	2,4	4,0	5,6	8,0	10,0	11,0	12,5
1000	3,2	5,0	3,2	5,0	7,1	10,0	12,5	14,0	16,0

Creepage Analyis advantages

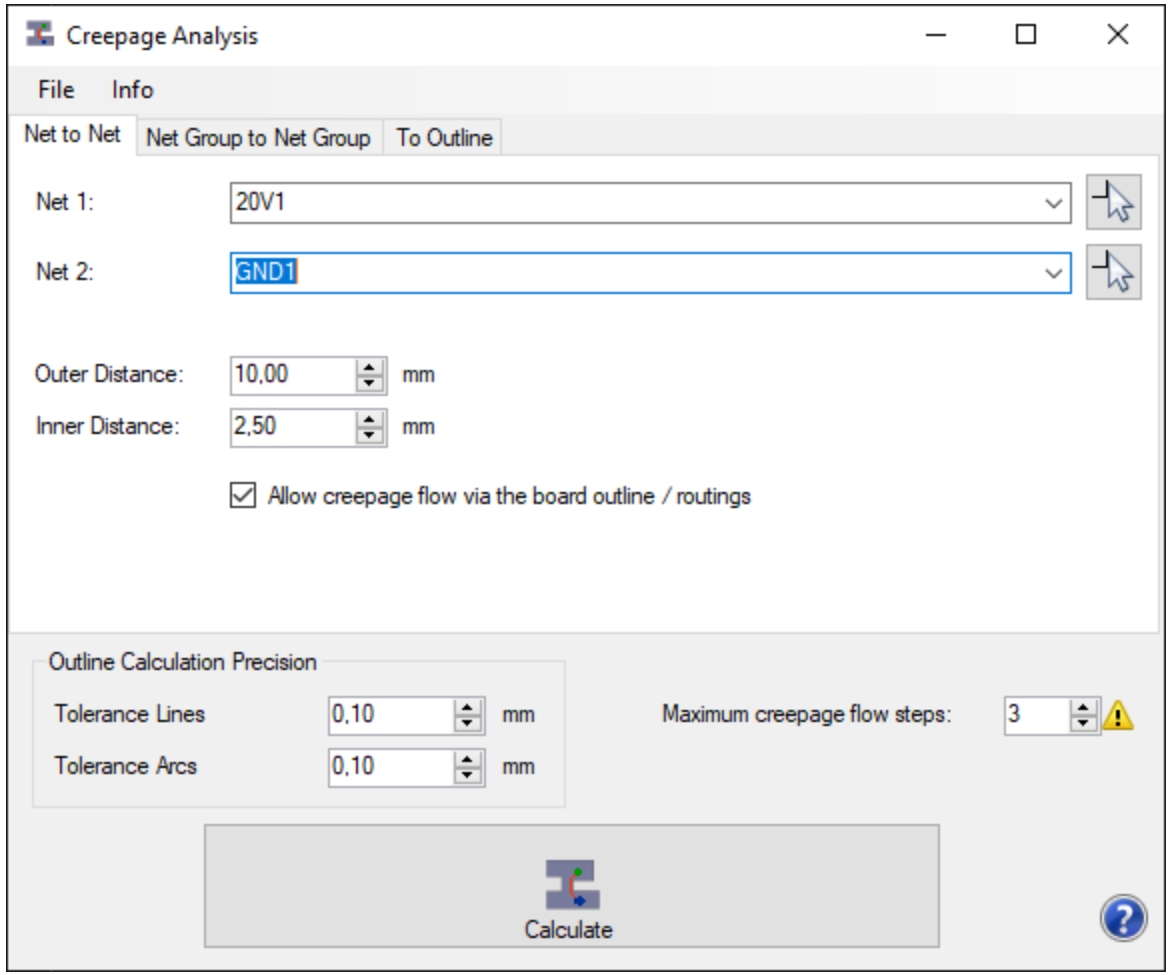




https://manual.pcb-investigator.com/pages/creepage_analysis

Creepage Analysis

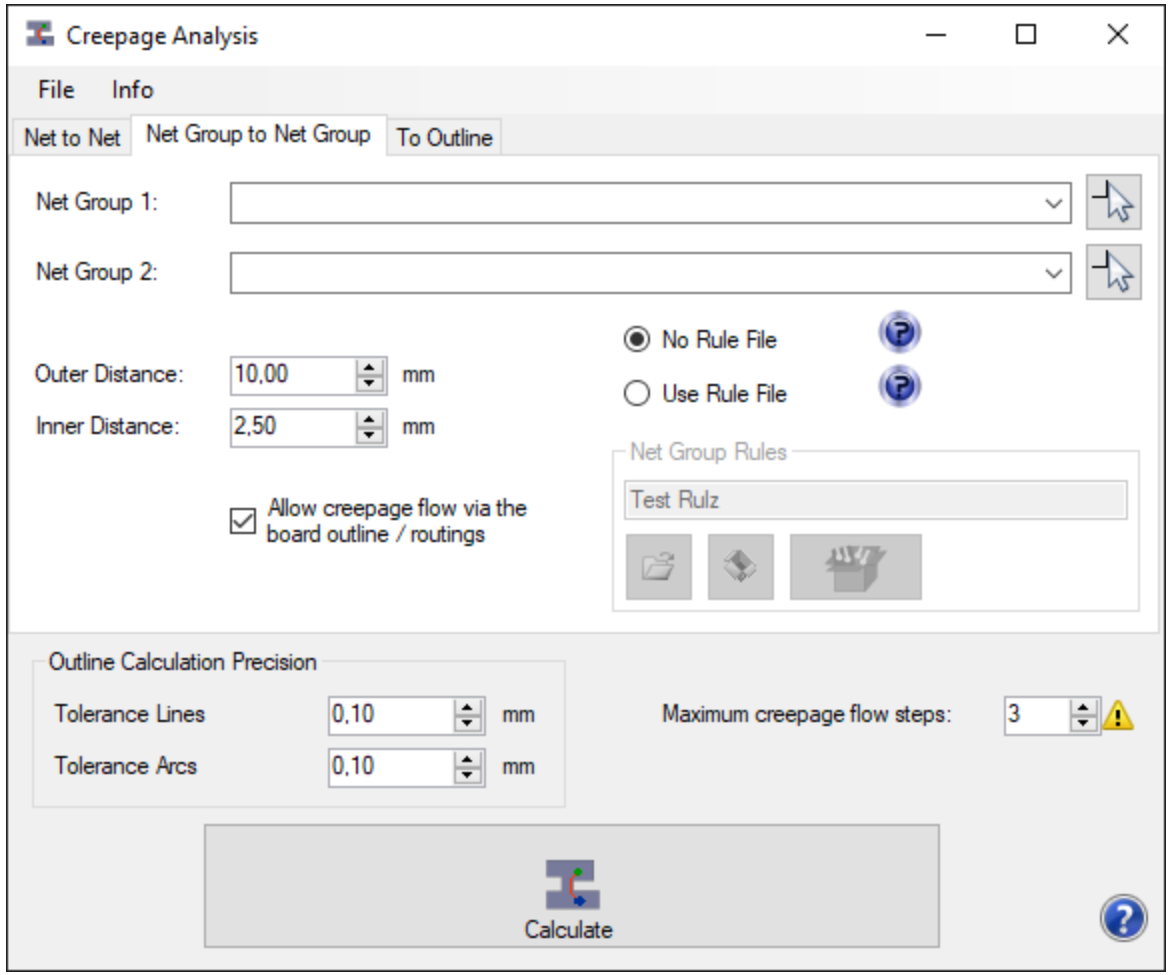
Net Mode



Net to Net creepage analysis is used to detect creepage issues between two single nets.

Creepage Analysis

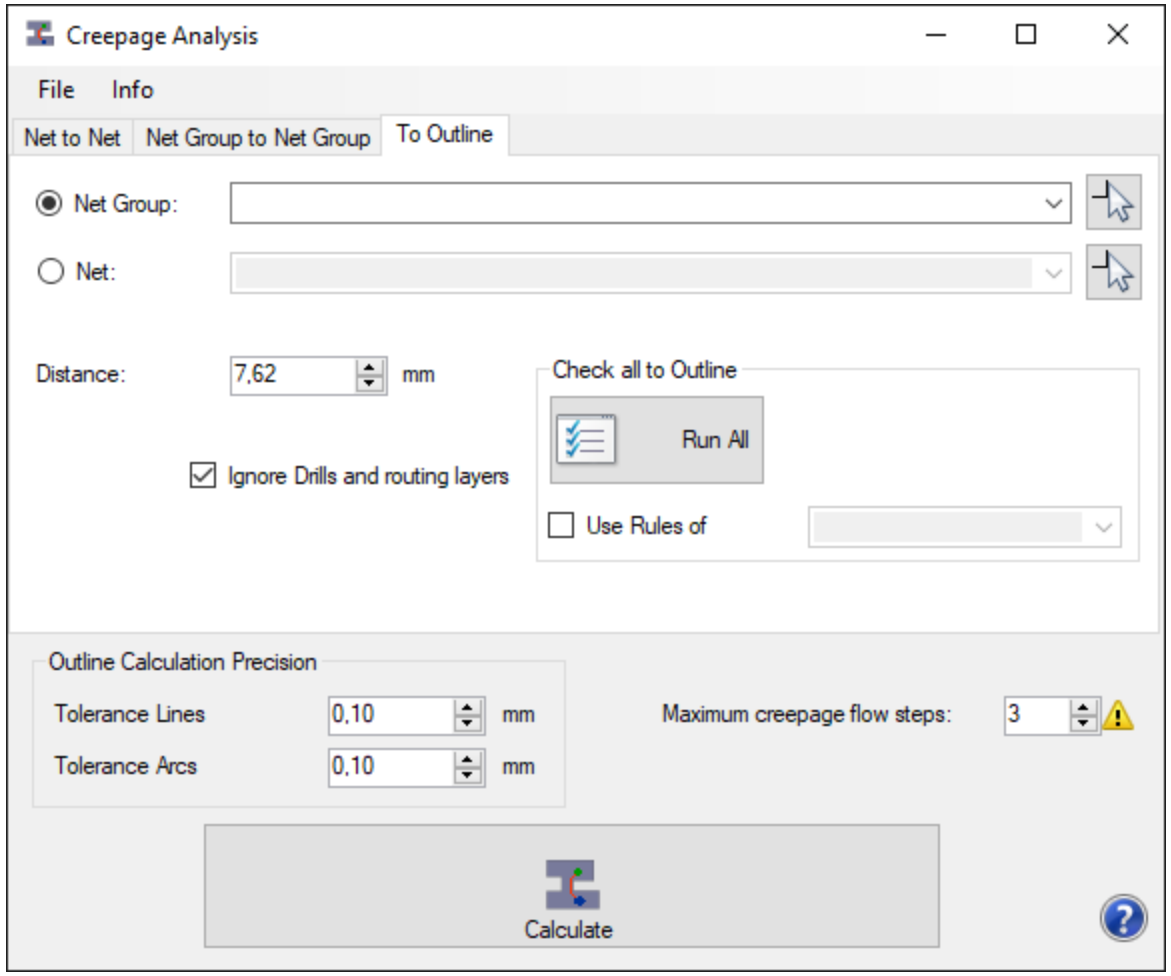
Net Group Mode



Net Group to Net Group creepage analysis has to be used to detect issues between any net of the first group to any net of the second group (*Note: You have to create Net Groups first. To create Net Groups use the button of the following image. Creating net groups can be found in "Net Groups", shown below)*

Creepage Analysis

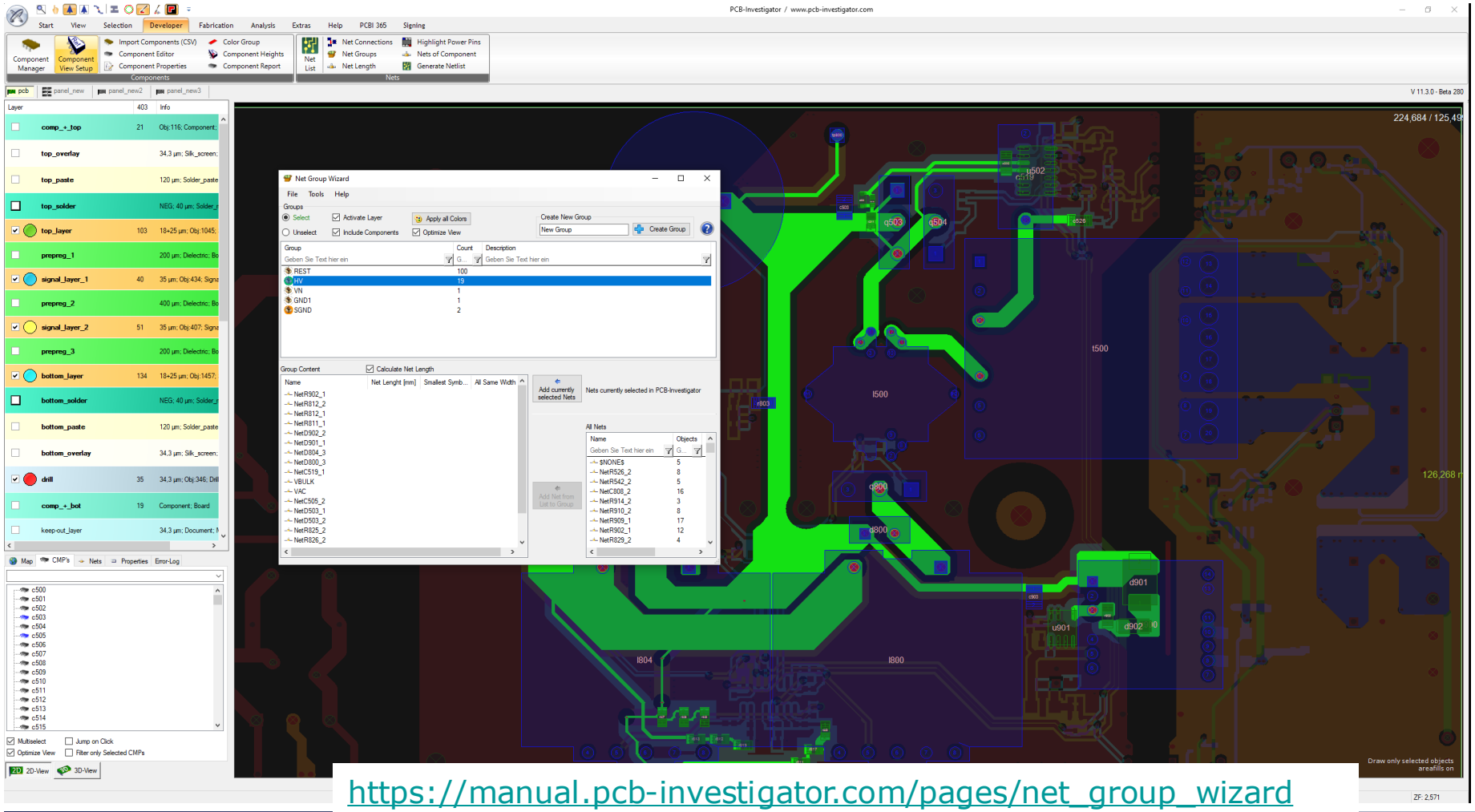
Outline Mode



There is also an option to detect issues between a single net, or any net of a group to the board outline of the PCB

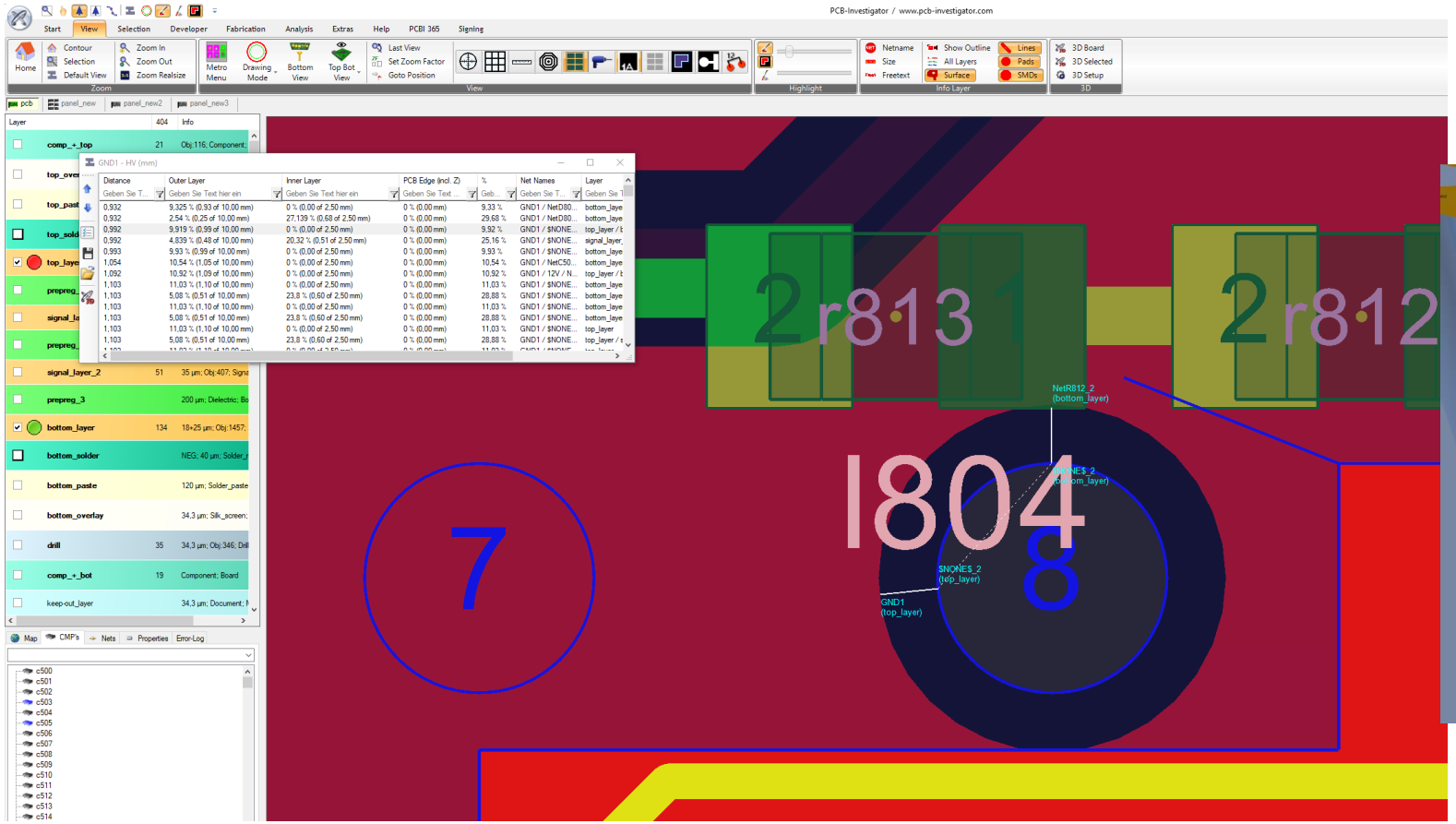
Creepage Analysis

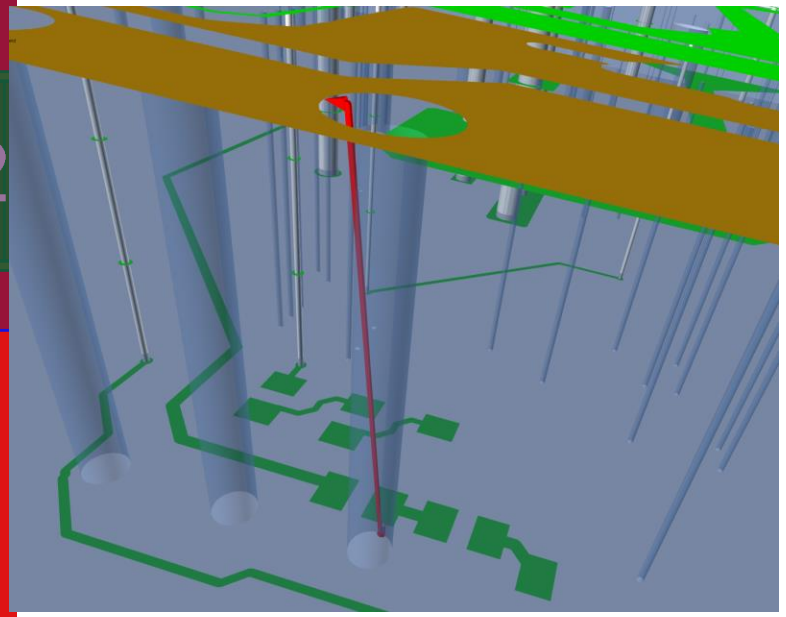
Preparing of Net Groups with the Net Group Wizard



https://manual.pcb-investigator.com/pages/net_group_wizard

Creepage Analysis





Hazard Analysis

Hazard analysis in PCB design is the process of identifying and assessing potential hazards that may arise from the use of a printed circuit board. There are several methods that can be used to perform hazard analysis, including:

1.Exposed copper analysis: This method involves comparing the non-lacquered, conductive copper pads and copper lines directly to each other. This type of simulation is more precise but takes longer to complete.

2.Solder mask opening analysis: This method involves comparing the solder mask openings (i.e., the surfaces not covered with varnish) rather than the copper pads and lines themselves. These areas are slightly larger than the copper areas they expose.

Both of these methods can help to identify potential hazards such as short circuits, electrical shocks, and component failure. By performing hazard analysis, engineers can design PCBs that are safer and more reliable for use.

Why using Hazard Analysis

There are several reasons why it is important to perform hazard analysis in the design of printed circuit boards (PCBs):

1. Safety: Hazard analysis helps to identify potential hazards that may arise from the use of a PCB, such as electrical shocks, short circuits, and component failure. By identifying and addressing these hazards, engineers can design safer PCBs.

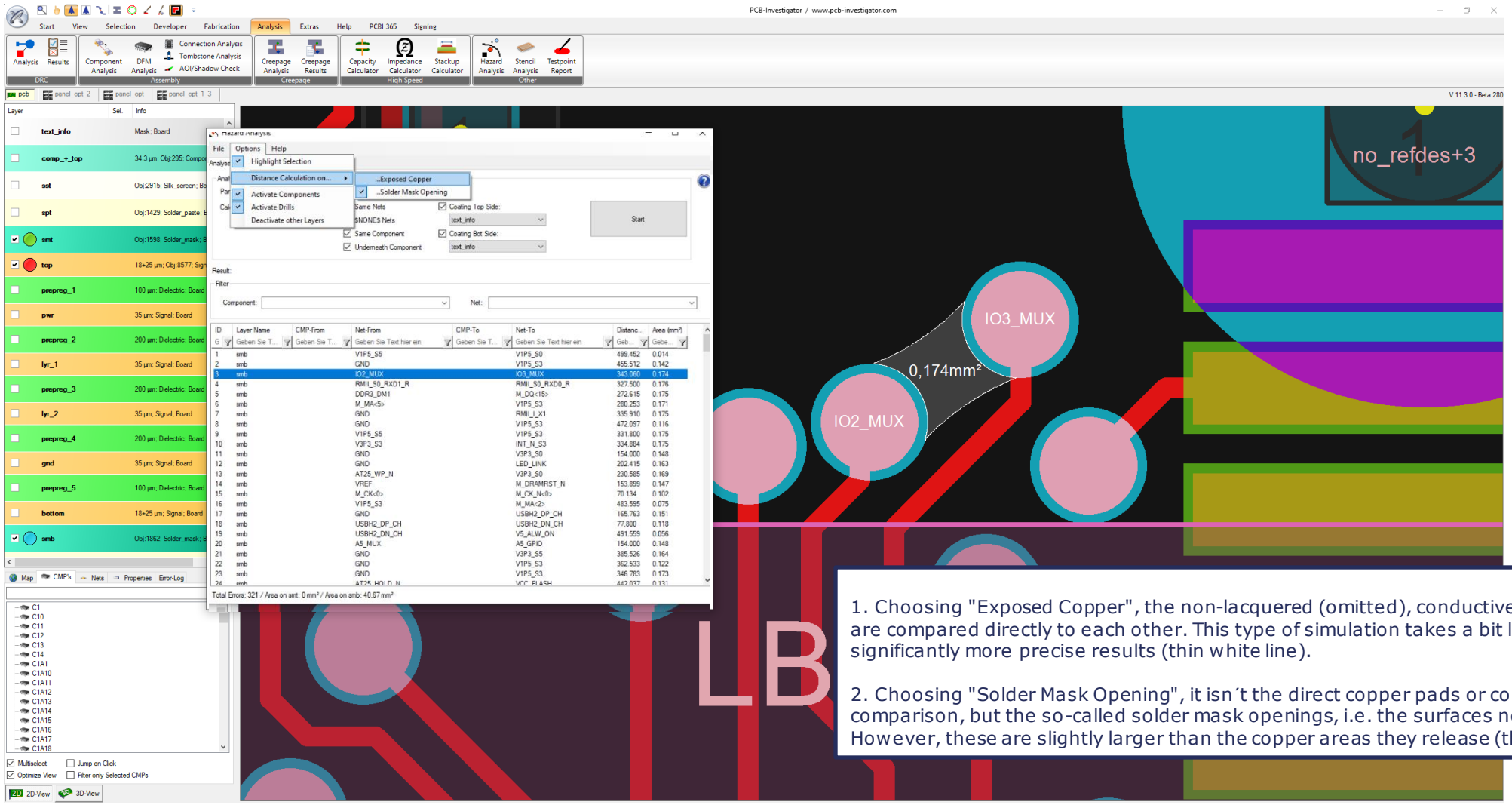
2. Reliability: Hazard analysis helps to identify areas of the PCB that may be prone to failure, such as areas with high current densities or areas where the insulation may break down. By addressing these issues during the design process, engineers can improve the reliability of the PCB.

3. Compliance: Many electrical and electronic products are required to meet certain safety and reliability standards. Hazard analysis is often used to ensure that these standards are met.

4. Cost-saving: By identifying and addressing potential hazards early in the design process, engineers can avoid costly redesigns or product recalls later on.

Overall, hazard analysis is an important step in the design process for PCBs because it helps to ensure the safety, reliability, and compliance of the final product.

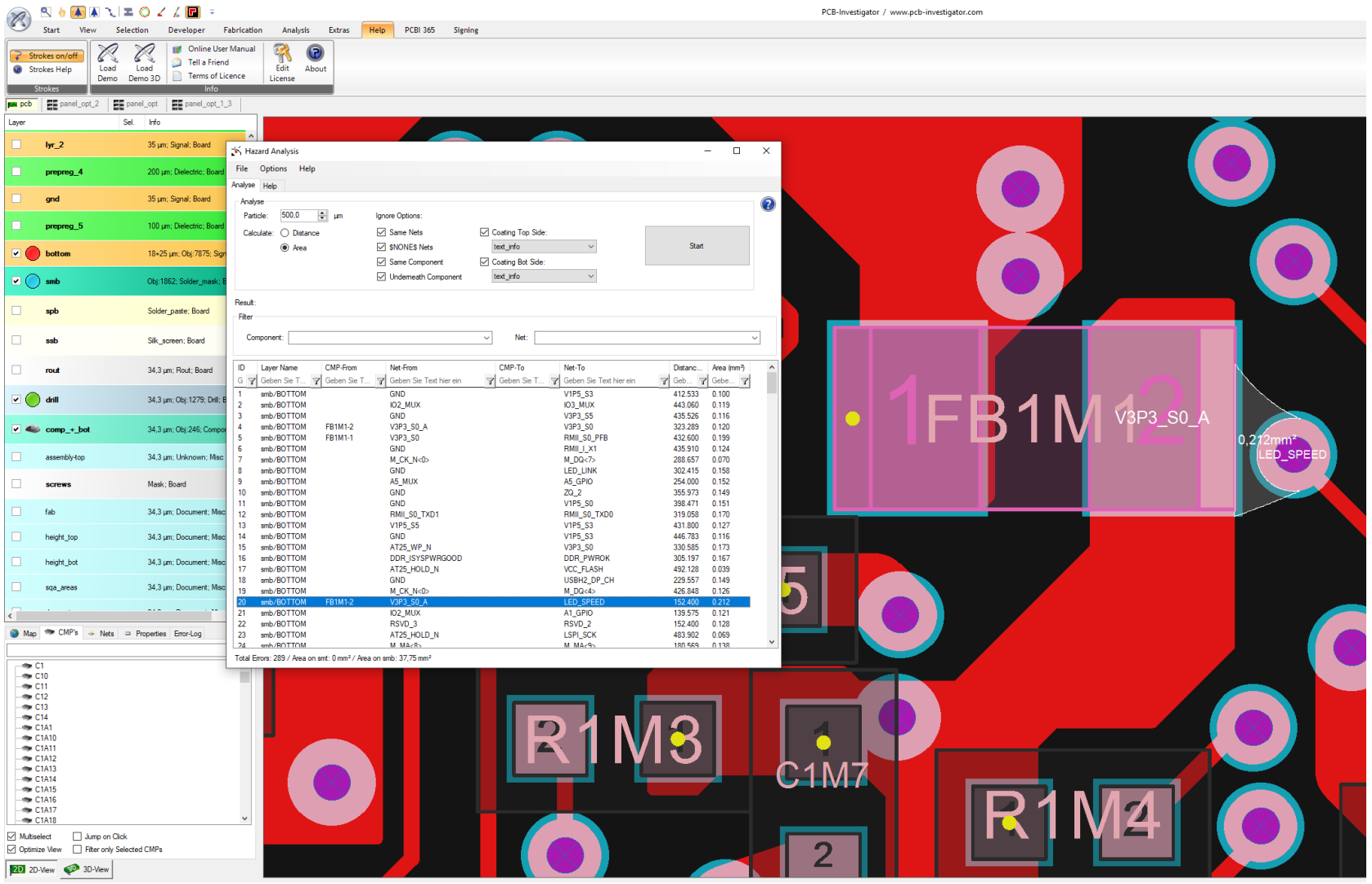
Hazard Analysis



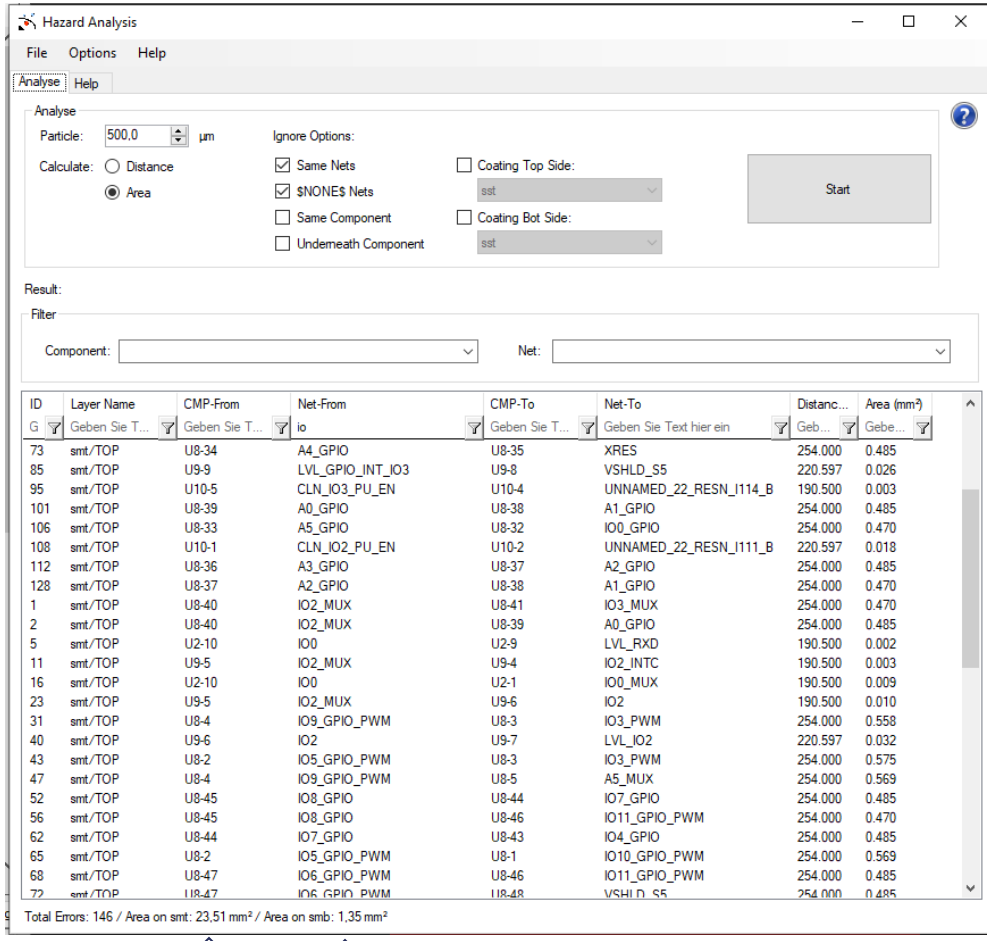
1. Choosing "Exposed Copper", the non-lacquered (omitted), conductive copper pads and copper lines are compared directly to each other. This type of simulation takes a bit longer but produces significantly more precise results (thin white line).

2. Choosing "Solder Mask Opening", it isn´t the direct copper pads or copper lines that are used for comparison, but the so-called solder mask openings, i.e. the surfaces not being covered with varnish. However, these are slightly larger than the copper areas they release (thick white line).

Hazard Analysis



Hazard Analysis

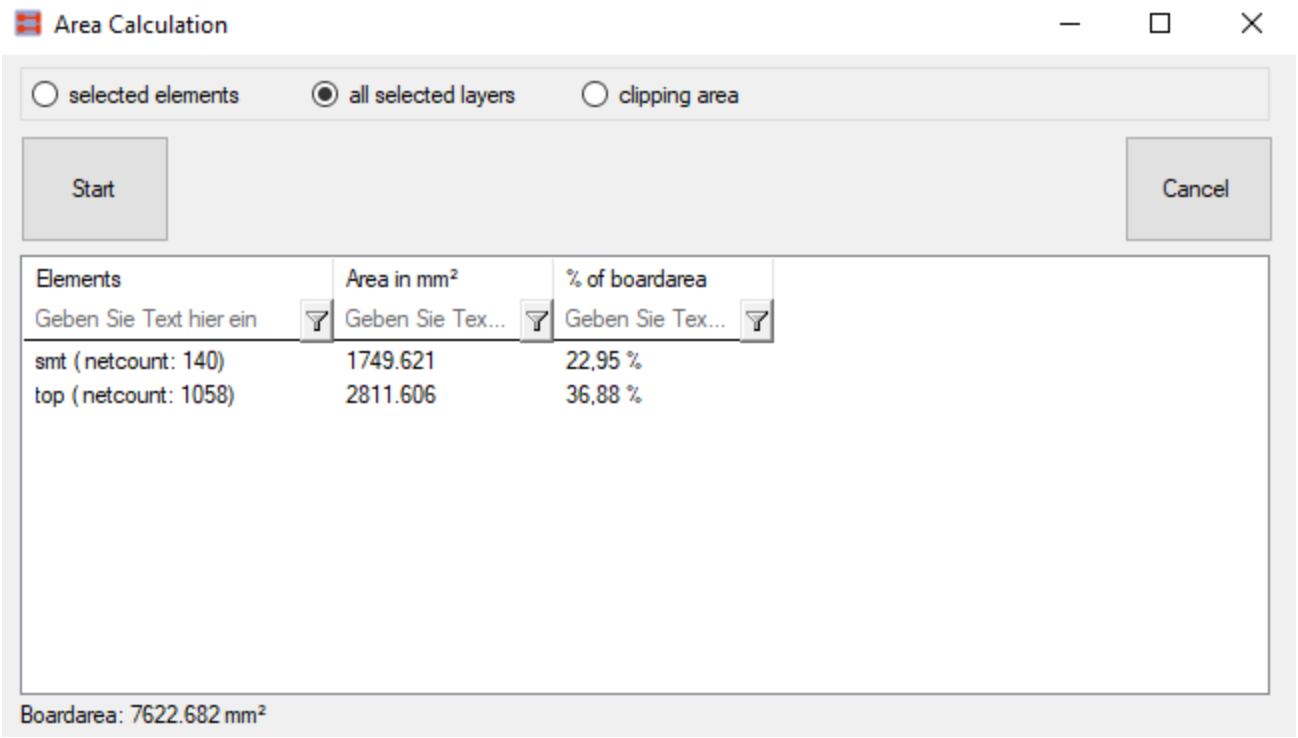


ID	Layer Name	CMP-From	Net-From	CMP-To	Net-To	Distanc...	Area (mm²)
73	smt/TOP	U8-34	A4_GPIO	U8-35	XRES	254.000	0.485
85	smt/TOP	U9-9	LVL_GPIO_INT_IO3	U9-8	VSHLD_S5	220.597	0.026
95	smt/TOP	U10-5	CLN_IO3_PU_EN	U10-4	UNNAMED_22_RESN_I114_B	190.500	0.003
101	smt/TOP	U8-39	A0_GPIO	U8-38	A1_GPIO	254.000	0.485
106	smt/TOP	U8-33	A5_GPIO	U8-32	IO0_GPIO	254.000	0.470
108	smt/TOP	U10-1	CLN_IO2_PU_EN	U10-2	UNNAMED_22_RESN_I111_B	220.597	0.018
112	smt/TOP	U8-36	A3_GPIO	U8-37	A2_GPIO	254.000	0.485
128	smt/TOP	U8-37	A2_GPIO	U8-38	A1_GPIO	254.000	0.470
1	smt/TOP	U8-40	IO2_MUX	U8-41	IO3_MUX	254.000	0.470
2	smt/TOP	U8-40	IO2_MUX	U8-39	A0_GPIO	254.000	0.485
5	smt/TOP	U2-10	IO0	U2-9	LVL_RXD	190.500	0.002
11	smt/TOP	U9-5	IO2_MUX	U9-4	IO2_INTC	190.500	0.003
16	smt/TOP	U2-10	IO0	U2-1	IO0_MUX	190.500	0.009
23	smt/TOP	U9-5	IO2_MUX	U9-6	IO2	190.500	0.010
31	smt/TOP	U8-4	IO9_GPIO_PWM	U8-3	IO3_PWM	254.000	0.558
40	smt/TOP	U9-6	IO2	U9-7	LVL_IO2	220.597	0.032
43	smt/TOP	U8-2	IO5_GPIO_PWM	U8-3	IO3_PWM	254.000	0.575
47	smt/TOP	U8-4	IO9_GPIO_PWM	U8-5	A5_MUX	254.000	0.569
52	smt/TOP	U8-45	IO8_GPIO	U8-44	IO7_GPIO	254.000	0.485
56	smt/TOP	U8-45	IO8_GPIO	U8-46	IO11_GPIO_PWM	254.000	0.470
62	smt/TOP	U8-44	IO7_GPIO	U8-43	IO4_GPIO	254.000	0.485
65	smt/TOP	U8-2	IO5_GPIO_PWM	U8-1	IO10_GPIO_PWM	254.000	0.569
68	smt/TOP	U8-47	IO6_GPIO_PWM	U8-46	IO11_GPIO_PWM	254.000	0.485
72	smt/TOP	U8-47	IO6_GPIO_PWM	U8-48	VSHLD_S5	254.000	0.485

surface without overlap

Hazard Analysis

Total Area of Board



Hazard Analysis

https://bauteilsauberkeit.zvei.org/en/risikoabschatzungstool.html

According to the ZVEI (Central Association of the Electrical and Electronics Industry), component cleanliness is calculated based on four criteria:

1. The number of particles per cm²
2. The size of the particles in micrometers
3. The number of particles per piece
4. The type of particles (e.g. metal, plastic, paper)

Component cleanliness is measured using cleanroom technology and specialized measuring methods. The results are then expressed in a cleanliness grade, which indicates the cleanliness of the component. The cleanliness grades are divided into classes from 1 to 9, with class 1 being the highest cleanliness and class 9 being the lowest cleanliness.
Component cleanliness is important in the electronics industry because it can directly affect the functionality and lifespan of electronic components. Cleanliness problems can lead to errors and failures in electronics products. Therefore, it is important to carefully measure and monitor component cleanliness.

Hazard Analysis

https://bauteilsauberkeit.zvei.org/en/risikoabschatzungstool.html

Extensions

Request Customized Functions

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Useful Links:

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