



EASYLOGIX.DE



PCB-Investigator

Creepage Analysis / Hazard Analysis

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Why Creepage Analysis is important

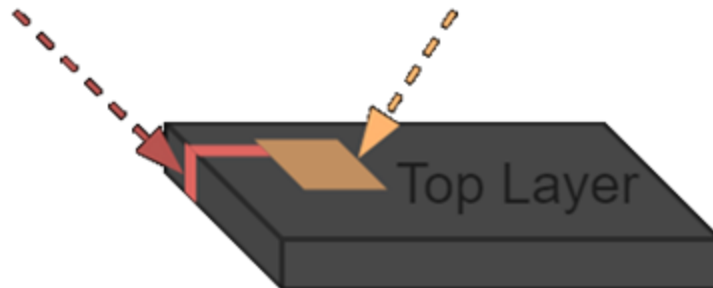
Creepage analysis is the study of the electrical path that a current follows on a printed circuit board (PCB) or other electrical component. It is important for several reasons:

- **Safety:** Creepage analysis helps to identify areas where electrical current may be able to jump across an insulating material, potentially causing a short circuit or electrical shock. By identifying these areas, engineers can design PCBs that are safer to use.
- **Reliability:** Creepage analysis helps to identify areas on a PCB where the electrical current may be able to break down the insulation, leading to component failure. By identifying these areas and designing accordingly, engineers can improve the reliability of the PCB.
- **Compliance:** Many electrical and electronic products are required to meet certain safety and reliability standards. Creepage analysis is often used to ensure that these standards are met.
- **In summary,** creepage analysis is important because it helps to ensure the safety, reliability, and compliance of electrical and electronic products.

Why Creepage Analysis is important

The **Creepage Analysis** in PCB-Investigator calculates the shortest distance from the outer edges to the conductive components to one another and to the outer edge of the board. This also considers uncoated drill holes (e.g. mount drill holes) and indentations, which otherwise would be too time consuming to calculate manually.

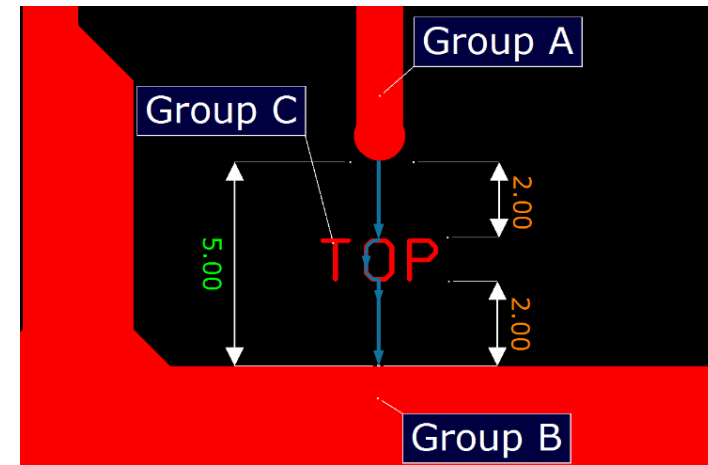
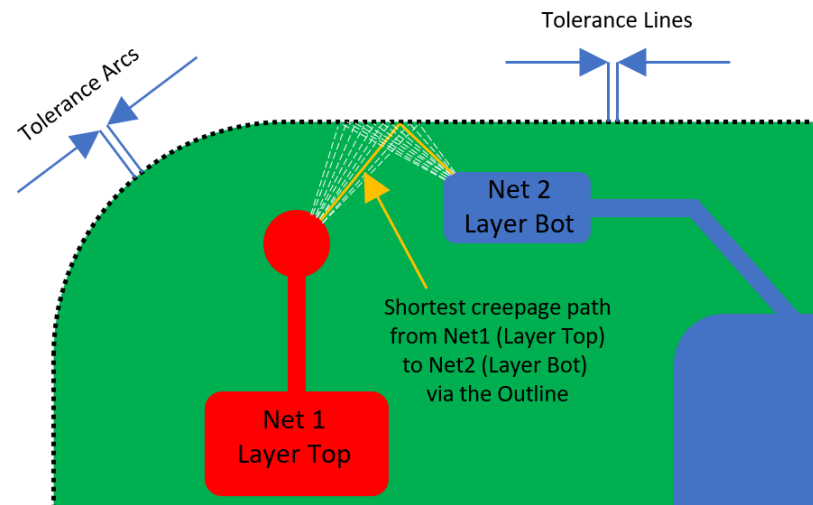
1. Net to Net creepage analysis is used to detect creepage issues between two single nets.
2. Net Group to Net Group creepage analysis has to be used to detect issues between any net of the first group to any net of thesecond group (Note: You have to create Net Groups first. To create Net Groups use the button of the following image. Creating net groups can be found in "Net Groups", shown below)
3. There is also an option to detect issues between a single net, or any net of a group to the board outline of the PCB



F.4 DIN EN 60664-1 (VDE 0110-1), table F.4 (extract)
Creepage distance for the avoidance of the failure by tracking

Voltage r.m.s. ¹⁾	Minimum creepage distances								
	Printed wiring material			Pollution degree					
	①	2	1	2			③		
	All material groups	All material groups except IIIb	All material groups	Material group I	Material group II	Material group III	Material group I	Material group II	Material group III ²⁾
V	mm	mm	mm	mm	mm	mm	mm	mm	mm
25	0,025	0,040	0,125	0,500	0,500	0,500	1,250	1,250	1,250
32	0,025	0,040	0,14	0,53	0,53	0,53	1,30	1,30	1,30
40	0,025	0,040	0,16	0,56	0,80	1,10	1,40	1,60	1,80
50	0,025	0,040	0,18	0,60	0,85	1,20	1,50	1,70	1,90
63	0,040	0,063	0,20	0,63	0,90	1,25	1,60	1,80	2,00
80	0,063	0,100	0,22	0,67	0,95	1,30	1,70	1,90	2,10
100	0,100	0,160	0,25	0,71	1,00	1,40	1,80	2,00	2,20
125	0,160	0,250	0,28	0,75	1,05	1,50	1,90	2,10	2,40
160	0,250	0,400	0,32	0,80	1,10	1,60	2,00	2,20	2,50
200	0,400	0,630	0,42	1,00	1,40	2,00	2,50	2,80	3,20
250	0,560	1,000	0,56	1,25	1,80	2,50	3,20	3,60	4,00
320	0,75	1,60	0,75	1,60	2,20	3,20	4,00	4,50	5,00
400	1,0	2,0	1,0	2,0	2,8	4,0	5,0	5,6	6,3
500	1,3	2,5	1,3	2,5	3,6	5,0	6,3	7,1	8,0
630	1,8	3,2	1,8	3,2	4,5	6,3	8,0	9,0	10,0
800	2,4	4,0	2,4	4,0	5,6	8,0	10,0	11,0	12,5
1000	3,2	5,0	3,2	5,0	7,1	10,0	12,5	14,0	16,0

Creepage Analysis advantages



https://manual.pcb-investigator.com/pages/creepage_analysis

Creepage Analysis

Net Mode

The screenshot shows the 'Creepage Analysis' window with the following settings:

- File Info
- Net to Net (selected), Net Group to Net Group, To Outline
- Net 1: 20V1
- Net 2: GND1
- Outer Distance: 10,00 mm
- Inner Distance: 2,50 mm
- Allow creepage flow via the board outline / routings
- Outline Calculation Precision:
 - Tolerance Lines: 0,10 mm
 - Tolerance Arcs: 0,10 mm
- Maximum creepage flow steps: 3
- Calculate button
- Help icon

Net to Net creepage analysis is used to detect creepage issues between two single nets.

Creepage Analysis

Net Group Mode

The screenshot shows the 'Creepage Analysis' window with the following settings:

- File Info: Net to Net, Net Group to Net Group, To Outline
- Net Group 1: [Empty dropdown]
- Net Group 2: [Empty dropdown]
- Outer Distance: 10,00 mm
- Inner Distance: 2,50 mm
- Radio buttons: No Rule File, Use Rule File
- Net Group Rules: Test Rulz
- Checkboxes: Allow creepage flow via the board outline / routings
- Outline Calculation Precision: Tolerance Lines 0,10 mm, Tolerance Arcs 0,10 mm
- Maximum creepage flow steps: 3
- Buttons: Calculate, ?

Net Group to Net Group creepage analysis has to be used to detect issues between any net of the first group to any net of the second group (*Note: You have to create Net Groups first. To create Net Groups use the button of the following image. Creating net groups can be found in "Net Groups", shown below*)

Creepage Analysis

Outline Mode

The screenshot shows the 'Creepage Analysis' window with the 'To Outline' tab selected. The interface includes the following elements:

- File Info** menu at the top.
- Three tabs: 'Net to Net', 'Net Group to Net Group', and 'To Outline'.
- Radio buttons for selection: 'Net Group' (selected) and 'Net'.
- A 'Distance' field set to '7,62 mm'.
- A checked checkbox for 'Ignore Drills and routing layers'.
- A 'Check all to Outline' section with a 'Run All' button and a 'Use Rules of' dropdown menu.
- An 'Outline Calculation Precision' section with 'Tolerance Lines' and 'Tolerance Arcs' both set to '0,10 mm'.
- A 'Maximum creepage flow steps' field set to '3' with a warning icon.
- A large 'Calculate' button at the bottom center.
- A help icon (question mark) at the bottom right.

There is also an option to detect issues between a single net, or any net of a group to the board outline of the PCB

Creepage Analysis

Preparing of Net Groups with the Net Group Wizard

The screenshot displays the PCB-Investigator software interface. The main window shows a PCB layout with various components and nets. A dialog box titled "Net Group Wizard" is open, allowing the user to create new net groups. The dialog includes a "Groups" section with a table of existing groups, a "Group Content" section with a table of net lengths, and a "Net Group Wizard" section with a table of net lengths.

Group	Count	Description
REST	100	
VW	1	
GND1	1	
SGND	2	

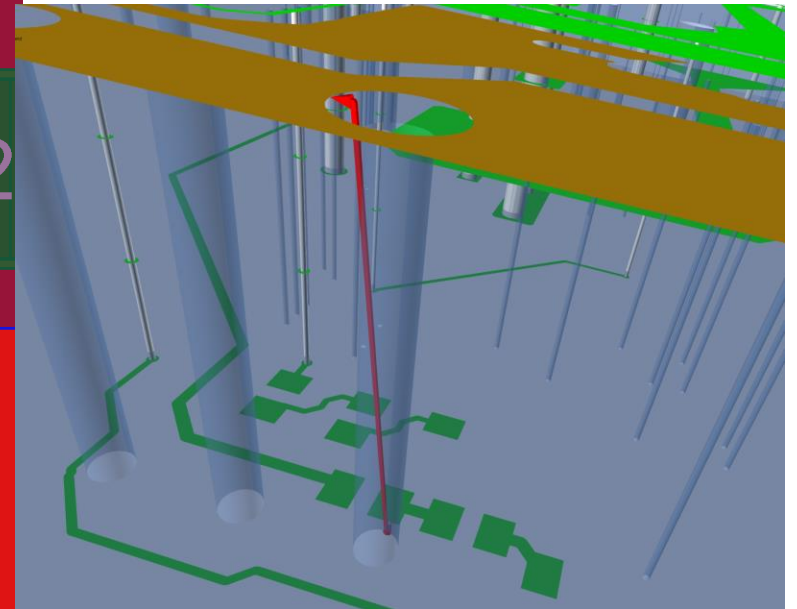
Name	Net Length [mm]	Smallest Symbol	All Same Width
NetR802_1			
NetR812_2			
NetR812_1			
NetR811_1			
NetD802_2			
NetD801_1			
NetD804_3			
NetD800_3			
NetC819_1			
VBLUK			
VAC			
NetC805_2			
NetD802_1			
NetD803_2			
NetR825_2			
NetR826_2			

Name	Objects
\$NONE\$	5
NetR808_2	8
NetR842_2	5
NetC808_2	16
NetR814_2	3
NetR810_2	8
NetR809_1	17
NetR802_1	12
NetR829_2	4

https://manual.pcb-investigator.com/pages/net_group_wizard

Creepage Analysis

Distance	Outer Layer	Inner Layer	PCB Edge Incl. Z	%	Net Names	Layer
Gaben Sie Text hier ein	Gaben Sie Text hier ein	Gaben Sie Text hier ein	Gaben Sie Text	Gab.	Gaben Sie T.	Gaben Sie
0.932	9.325 % (0.93 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	9.33 %	GND1 / NetD80	bottom_layer
0.932	2.54 % (0.25 of 10.00 mm)	27.139 % (0.68 of 2.50 mm)	0 % (0.00 mm)	29.68 %	GND1 / NetD80	bottom_layer
0.992	9.919 % (0.99 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	9.92 %	GND1 / SHONE	top_layer / t
0.992	4.839 % (0.48 of 10.00 mm)	20.32 % (0.51 of 2.50 mm)	0 % (0.00 mm)	25.16 %	GND1 / SHONE	signal_layer
0.993	9.93 % (0.99 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	9.93 %	GND1 / SHONE	bottom_layer
1.054	10.54 % (1.05 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	10.54 %	GND1 / NetC50	bottom_layer
1.092	10.92 % (1.09 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	10.92 %	GND1 / 12V / N	top_layer / t
1.103	11.03 % (1.10 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	11.03 %	GND1 / SHONE	bottom_layer
1.103	5.08 % (0.51 of 10.00 mm)	23.8 % (0.60 of 2.50 mm)	0 % (0.00 mm)	28.88 %	GND1 / SHONE	bottom_layer
1.103	11.03 % (1.10 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	11.03 %	GND1 / SHONE	top_layer
1.103	5.08 % (0.51 of 10.00 mm)	23.8 % (0.60 of 2.50 mm)	0 % (0.00 mm)	28.88 %	GND1 / SHONE	top_layer / t
1.103	11.03 % (1.10 of 10.00 mm)	0 % (0.00 of 2.50 mm)	0 % (0.00 mm)	11.03 %	GND1 / SHONE	bottom_layer



Hazard Analysis

Hazard analysis in PCB design is the process of identifying and assessing potential hazards that may arise from the use of a printed circuit board. There are several methods that can be used to perform hazard analysis, including:

- 1.Exposed copper analysis: This method involves comparing the non-lacquered, conductive copper pads and copper lines directly to each other. This type of simulation is more precise but takes longer to complete.
- 2.Solder mask opening analysis: This method involves comparing the solder mask openings (i.e., the surfaces not covered with varnish) rather than the copper pads and lines themselves. These areas are slightly larger than the copper areas they expose.

Both of these methods can help to identify potential hazards such as short circuits, electrical shocks, and component failure. By performing hazard analysis, engineers can design PCBs that are safer and more reliable for use.

Why using Hazard Analysis

There are several reasons why it is important to perform hazard analysis in the design of printed circuit boards (PCBs):

1. **Safety:** Hazard analysis helps to identify potential hazards that may arise from the use of a PCB, such as electrical shocks, short circuits, and component failure. By identifying and addressing these hazards, engineers can design safer PCBs.
2. **Reliability:** Hazard analysis helps to identify areas of the PCB that may be prone to failure, such as areas with high current densities or areas where the insulation may break down. By addressing these issues during the design process, engineers can improve the reliability of the PCB.
3. **Compliance:** Many electrical and electronic products are required to meet certain safety and reliability standards. Hazard analysis is often used to ensure that these standards are met.
4. **Cost-saving:** By identifying and addressing potential hazards early in the design process, engineers can avoid costly redesigns or product recalls later on.

Overall, hazard analysis is an important step in the design process for PCBs because it helps to ensure the safety, reliability, and compliance of the final product.

Hazard Analysis

PCB-Investigator / www.pcb-investigator.com

V 11.3.0 - Beta 200

no_refdes+3

IO3_MUX
0,174mm²
IO2_MUX

ID	Layer Name	CMP-From	Net-From	CMP-To	Net-To	Distanc...	Area (mm ²)
1	smb	V1P5_S5	V1P5_S0	V1P5_S3	V1P5_S3	499.452	0.014
2	smb	GND	GND	V1P5_S3	V1P5_S3	455.512	0.142
4	smb	V3P3_S0	V3P3_S0	V3P3_S0	V3P3_S0	327.500	0.175
5	smb	RMI1_S0_RXD0_L	RMI1_S0_RXD0_R	M_DO-15>	M_DO-15>	272.615	0.175
6	smb	M_MA<5>	V1P5_S3	V1P5_S3	V1P5_S3	280.253	0.171
7	smb	GND	GND	RMI1_X1	RMI1_X1	335.910	0.175
8	smb	V1P5_S3	V1P5_S3	V1P5_S3	V1P5_S3	472.097	0.116
9	smb	V1P5_S5	V1P5_S3	V1P5_S3	V1P5_S3	331.800	0.175
10	smb	V3P3_S3	INT_N_S3	INT_N_S3	INT_N_S3	334.884	0.175
11	smb	GND	V3P3_S0	V3P3_S0	V3P3_S0	154.000	0.148
12	smb	GND	GND	LED_LINK	LED_LINK	202.415	0.163
13	smb	AT25_WP_N	V3P3_S0	V3P3_S0	V3P3_S0	230.585	0.169
14	smb	VREF	M_DRAMRST_N	M_DRAMRST_N	M_DRAMRST_N	153.899	0.147
15	smb	M_CK<0>	M_CK_N<0>	M_CK_N<0>	M_CK_N<0>	70.134	0.102
16	smb	V1P5_S3	M_MA<2>	M_MA<2>	M_MA<2>	483.595	0.075
17	smb	GND	USBH2_DP_CH	USBH2_DP_CH	USBH2_DP_CH	165.763	0.151
18	smb	USBH2_DP_CH	USBH2_DP_CH	USBH2_DP_CH	USBH2_DP_CH	77.800	0.118
19	smb	USBH2_DN_CH	V5_ALW_ON	V5_ALW_ON	V5_ALW_ON	491.559	0.056
20	smb	AS_MUX	AS_GPI0	AS_GPI0	AS_GPI0	154.000	0.148
21	smb	GND	V0P3_S5	V0P3_S5	V0P3_S5	365.526	0.164
22	smb	GND	V1P5_S3	V1P5_S3	V1P5_S3	362.533	0.122
23	smb	GND	V1P5_S3	V1P5_S3	V1P5_S3	346.783	0.173
24	smb	AT25_H010_N	VCC_FLASH	VCC_FLASH	VCC_FLASH	442.037	0.131

Total Errors: 321 / Area on smt: 0mm² / Area on smb: 40,67mm²

1. Choosing "Exposed Copper", the non-lacquered (omitted), conductive copper pads and copper lines are compared directly to each other. This type of simulation takes a bit longer but produces significantly more precise results (thin white line).

2. Choosing "Solder Mask Opening", it isn't the direct copper pads or copper lines that are used for comparison, but the so-called solder mask openings, i.e. the surfaces not being covered with varnish. However, these are slightly larger than the copper areas they release (thick white line).

Hazard Analysis

PCB-Investigator / www.pcb-investigator.com

Strokes on/off, Strokes Help, Load Demo, Load Demo 3D, Online User Manual, Tell a Friend, Terms of Licence, Edit, About

Layer: pcb, panel_opt_2, panel_opt, panel_opt_1_3

Layer List:

- lyr_2: 35 µm; Signal; Board
- prepreg_4: 200 µm; Dielectric; Board
- grnd: 35 µm; Signal; Board
- prepreg_5: 100 µm; Dielectric; Board
- bottom: 18-25 µm; Obj: 7875; Signal; Board
- smb: Obj: 1862; Solder_mask; Board
- spb: Solder_paste; Board
- ssb: Silk_screen; Board
- rout: 34.3 µm; Rout; Board
- drill: 34.3 µm; Obj: 1279; Drill; Board
- comp_+_bot: 34.3 µm; Obj: 246; Component; Board
- assembly_top: 34.3 µm; Unknown; Mask; Board
- screws: Mask; Board
- fab: 34.3 µm; Document; Mask; Board
- height_top: 34.3 µm; Document; Mask; Board
- height_bot: 34.3 µm; Document; Mask; Board
- sqa_areas: 34.3 µm; Document; Mask; Board

Hazard Analysis Window:

Analyse: Particle: 500.0 µm, Ignore Options: Same Nets, \$NONES Nets, Same Component, Undereath Component, Coating Top Side, Coating Bot Side, text_info

Calculate: Distance, Area

Result:

ID	Layer Name	CMP-From	Net-From	CMP-To	Net-To	Distanc...	Area (mm²)
1	smb/BOTTOM		GND		VIP5_S3		412.533
2	smb/BOTTOM		IO2_MUX		IO3_MUX		443.060
3	smb/BOTTOM		GND		V3P3_S5		435.526
4	smb/BOTTOM	FB1M1-2	V3P3_S0_A		V3P3_S0		323.289
5	smb/BOTTOM	FB1M1-1	V3P3_S0		RMI_S0_PFB		432.600
6	smb/BOTTOM		GND		RMI_L_X1		435.910
7	smb/BOTTOM		M_CK_N<d>		M_DQ<7>		288.657
8	smb/BOTTOM		GND		LED_LINK		302.415
9	smb/BOTTOM		A5_MUX		A5_GPIO		254.000
10	smb/BOTTOM		GND		Z0_2		355.973
11	smb/BOTTOM		GND		VIP5_S0		398.471
12	smb/BOTTOM		RMI_S0_TXD1		RMI_S0_TXD0		319.058
13	smb/BOTTOM		VIP5_S5		VIP5_S3		431.800
14	smb/BOTTOM		GND		VIP5_S3		446.783
15	smb/BOTTOM		AT25_WP_N		V3P3_S0		330.585
16	smb/BOTTOM		DDR_J5SPWRGOOD		DDR_PWROK		305.197
17	smb/BOTTOM		AT25_HOLD_N		VCC_FLASH		492.128
18	smb/BOTTOM		GND		USBH2_DP_CH		229.557
19	smb/BOTTOM		M_CK_N<d>		M_DQ<4>		426.848
20	smb/BOTTOM	FB1M1-2	V3P3_S0_A		LED_SPEED		152.400
21	smb/BOTTOM		IO2_MUX		A1_GPIO		139.575
22	smb/BOTTOM		RSVD_3		RSVD_2		152.400
23	smb/BOTTOM		AT25_HOLD_N		LSPI_SCK		483.902
24	smb/BOTTOM		M_MA<5>		M_MA<4>		191.568

Total Errors: 289 / Area on smt: 0 mm² / Area on smb: 37,75 mm²

Hazard Analysis

Hazard Analysis

File Options Help

Analyse Help

Analyse

Particle: 500.0 μm

Calculate: Distance Area

Ignore Options:

Same Nets Coating Top Side: sst

\$NONES Nets Coating Bot Side: sst

Same Component Underneath Component

Start

Result:

Filter

Component: Net:

ID	Layer Name	CMP-From	Net-From	CMP-To	Net-To	Distanc...	Area (mm ²)
73	smt/TOP	U8-34	A4_GPIO	U8-35	XRES	254.000	0.485
85	smt/TOP	U9-9	LVL_GPIO_INT_IO3	U9-8	VSHLD_S5	220.597	0.026
95	smt/TOP	U10-5	CLN_IO3_PU_EN	U10-4	UNNAMED_22_RESN_I114_B	190.500	0.003
101	smt/TOP	U8-39	A0_GPIO	U8-38	A1_GPIO	254.000	0.485
106	smt/TOP	U8-33	A5_GPIO	U8-32	IO0_GPIO	254.000	0.470
108	smt/TOP	U10-1	CLN_IO2_PU_EN	U10-2	UNNAMED_22_RESN_I111_B	220.597	0.018
112	smt/TOP	U8-36	A3_GPIO	U8-37	A2_GPIO	254.000	0.485
128	smt/TOP	U8-37	A2_GPIO	U8-38	A1_GPIO	254.000	0.470
1	smt/TOP	U8-40	IO2_MUX	U8-41	IO3_MUX	254.000	0.470
2	smt/TOP	U8-40	IO2_MUX	U8-39	A0_GPIO	254.000	0.485
5	smt/TOP	U2-10	IO0	U2-9	LVL_RXD	190.500	0.002
11	smt/TOP	U9-5	IO2_MUX	U9-4	IO2_INTC	190.500	0.003
16	smt/TOP	U2-10	IO0	U2-1	IO0_MUX	190.500	0.009
23	smt/TOP	U9-5	IO2_MUX	U9-6	IO2	190.500	0.010
31	smt/TOP	U8-4	IO9_GPIO_PWM	U8-3	IO3_PWM	254.000	0.558
40	smt/TOP	U9-6	IO2	U9-7	LVL_IO2	220.597	0.032
43	smt/TOP	U8-2	IO5_GPIO_PWM	U8-3	IO3_PWM	254.000	0.575
47	smt/TOP	U8-4	IO9_GPIO_PWM	U8-5	A5_MUX	254.000	0.569
52	smt/TOP	U8-45	IO8_GPIO	U8-44	IO7_GPIO	254.000	0.485
56	smt/TOP	U8-45	IO8_GPIO	U8-46	IO11_GPIO_PWM	254.000	0.470
62	smt/TOP	U8-44	IO7_GPIO	U8-43	IO4_GPIO	254.000	0.485
65	smt/TOP	U8-2	IO5_GPIO_PWM	U8-1	IO10_GPIO_PWM	254.000	0.569
68	smt/TOP	U8-47	IO6_GPIO_PWM	U8-46	IO11_GPIO_PWM	254.000	0.485
72	smt/TOP	U8-47	IO6_GPIO_PWM	U8-48	VSHLD_S5	254.000	0.485

Total Errors: 146 / Area on smt: 23.51 mm² / Area on smb: 1.35 mm²

surface without overlap

Hazard Analysis

Total Area of Board

Area Calculation

selected elements all selected layers clipping area

Start Cancel

Elements	Area in mm ²	% of boardarea
Geben Sie Text hier ein	Geben Sie Tex...	Geben Sie Tex...
smt (netcount: 140)	1749.621	22,95 %
top (netcount: 1058)	2811.606	36,88 %

Boardarea: 7622.682 mm²

Hazard Analysis

<https://bauteilsauberkeit.zvei.org/en/risikoabschätzungstool.html>

According to the ZVEI (Central Association of the Electrical and Electronics Industry), component cleanliness is calculated based on four criteria:

- 1.The number of particles per cm²
- 2.The size of the particles in micrometers
- 3.The number of particles per piece
- 4.The type of particles (e.g. metal, plastic, paper)

Component cleanliness is measured using cleanroom technology and specialized measuring methods. The results are then expressed in a cleanliness grade, which indicates the cleanliness of the component. The cleanliness grades are divided into classes from 1 to 9, with class 1 being the highest cleanliness and class 9 being the lowest cleanliness.

Component cleanliness is important in the electronics industry because it can directly affect the functionality and lifespan of electronic components. Cleanliness problems can lead to errors and failures in electronics products. Therefore, it is important to carefully measure and monitor component cleanliness.

Hazard Analysis

<https://bauteilsauberkeit.zvei.org/en/risikoabschätzungstool.html>



Risikoabschätzungstool

Historie

Handbuch

Das ZVEI Risikoabschätzungstool zur Bestimmung des Kurzschlussrisikos durch Partikel

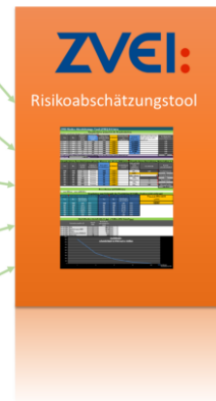
Partikelanzahl pro
Größenklasse

Kritische Fläche pro
Größenklasse

Gesamtinnenfläche

Einbaulage

Gewichtungsfaktoren



Kurzschluss-
wahrscheinlichkeit
in ppm

Derzeit finden sich in Bauteilspezifikationen oft Partikelgrenzwerte, die vom kleinsten elektrischen Abstand zwischen zwei stromführenden Bereichen abgeleitet sind. Dies führt dazu, dass extrem scharfe Anforderungen zugrunde liegen, die einerseits technisch und wirtschaftlich nicht umzusetzen sind und andererseits für das Risiko der Baugruppe in Richtung elektrischem Kurzschluss nicht notwendig sind.

Wie schon im Leitfaden beschrieben bietet der Arbeitskreis mit Hilfe des Risikoabschätzungstool eine Möglichkeit die Ausfallwahrscheinlichkeit (in ppm) einer Baugruppe anhand von durchgeführten TecSa-Analysen zu bewerten. Die Zielsetzung des Risikoabschätzungstools ist die Sauberkeit des Produktes "so sauber wie nötig" zu bestimmen und nicht "so sauber wie möglich", damit keine unnötigen Kosten generiert werden.

Auf dieser Seite finden Sie einen direkten Link zu dem webbasierten Tool sowie ein Handbuch, das Sie durch das Tool mit Hinweisen und Vorschlägen leitet.

- [Tool-Handbuch](#)
- [Historische und inhaltliche Zusammenfassung](#)

Berechnung durchführen

Extensions

Request Customized Functions

Get in touch,
info@easylogix.de

Useful Links:

PCB-Investigator
www.pcb-investigator.com

PCBi-Physics
www.PCBi-Physics.com

Native Board Import (3D Interface to CATIA, SiemensNX, SolidWorks, SolidEdge)
www.sts-development.biz

GerberLogix
www.gerberLogix.com

Online Gerber Viewer
www.Gerber-Viewer.com

Software Development, CAD Converter, data connection
www.easylogix.de